U.S. ATLAS PROJECT OFFICE

Physics Department
UPTON, NEW YORK 11973

October 11, 2001

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Dr. Thomas Kirk
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SUBJECT: U.S. ATLAS Project Monthly Status Report for August 2001

Dear Sirs:

Attached please find Monthly Status Report No. 42 for the U.S. ATLAS Project.

Sincerely yours,

William J. Willis
U.S. ATLAS Project Manager

Distribution:

Abolins, M.
Alam, S.
Baker, K.
Barnett, M.
Bensinger, J.
Blair, R.
Butehorn, C.
Carolan, P. - DOE
Cleland, W.
Crawford, G.
Cullen, J. – PAP
De, K.
Dodd, J.
Ernst, R.
Errede, S.
Feldman, G.
Gilchriese, M.
Goldberg, M. - NSF
Gordon, H.
Firestone, A. - NSF
Harrison, M. – PAP
Hinchliffe, I.
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Sinkular, M., NSF
Skubic, P.
Slattery, P.
Sliwa, K.
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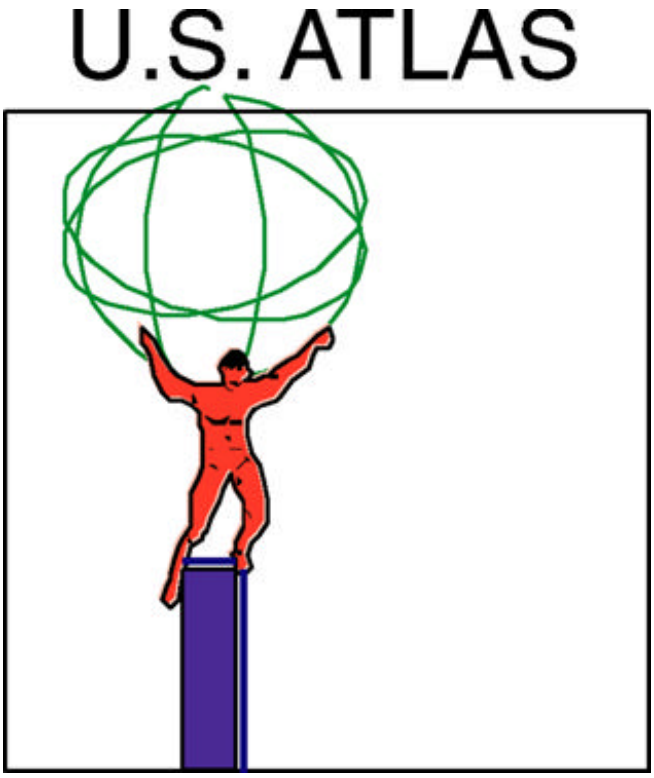
Whitaker, S.
Wolbers, S. - PAP
Williams, H.
Willis, W.
Wu, S.L.
Yeck, J.



PROJECT STATUS REPORT NO. 42

REPORTING PERIOD

AUGUST 2001

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1. PROJECT OBJECTIVE

The U.S. ATLAS Project consists of the activities to design, supply, install and commission the U.S. portion of the ATLAS detector. The detector will become part of the Large Hadron Collider (LHC) at CERN, the European Laboratory for Particle Physics. The ATLAS detector is being designed to understand the dynamics of electroweak symmetry breaking. The U.S. ATLAS collaboration is funded jointly by the U.S. Department of Energy and the National Science Foundation.

The fundamental unanswered problem of elementary particle physics relates to the understanding of the mechanism that generates the masses of the W and Z gauge bosons and of quarks and leptons. To attack this problem, one requires an experiment that can produce a large rate of particle collisions of very high energy. The LHC will collide protons against protons every 25 ns with a center-of-mass energy of 14 TeV and a design luminosity of 10^{34} cm^{-2} s^{-1}. It will probably require a few years after turn-on to reach the full design luminosity.

The detector will have to be capable of reconstructing the interesting final states. It must be designed to fully utilize the high luminosity so that detailed studies of rare phenomena can be carried out. While the primary goal of the experiment is to determine the mechanism of electroweak symmetry breaking via the detection of Higgs bosons, supersymmetric particles or structure in the WW scattering amplitude, the new energy regime will also offer the opportunity to probe for quark substructure or discover new exotic particles. The detector must be sufficiently versatile to detect and identify the final state products of these processes. In particular, it must be capable of reconstructing the momenta and directions of quarks (hadronic jets, tagged by their flavors where possible), electrons, muons, taus, and photons, and be sensitive to energy carried off by weakly interacting particles such as neutrinos that cannot be directly detected. The ATLAS detector will have all of these capabilities.

The ATLAS detector is expected to operate for twenty or more years at the CERN LHC, observing collisions of protons, and recording more than 10^7 events per year. The critical objectives to achieve these goals are:

- Excellent photon and electron identification capability, as well as energy and directional resolution.
- Efficient charged particle track reconstruction and good momentum resolution.
- Excellent muon identification capability and momentum resolution.
- Well-understood trigger system to go from 1 GHz raw interaction rate to ~100 Hz readout rate without loss of interesting signals.
- Hermetic calorimetry coverage to allow accurate measurement of direction and magnitude of energy flow, and excellent reconstruction of missing transverse momentum.
- Efficient tagging of b-decays and b-jets.

The U.S. ATLAS cost objective is $163.75M while supplying initially the work scope described in Appendix 3 of the Project Management Plan (PMP) and, if possible, all the goals described in Appendix 2 of the PMP.

The ATLAS project was initiated in FY 1996, and is scheduled for a 10-year design and fabrication period beginning in the first quarter of FY 1996, and finishing in FY 2005. This period will be followed by operation at the LHC.

2. TECHNICAL APPROACH CHANGES

No change.

3. PROJECT MANAGER'S SUMMARY ASSESSMENT – W. Willis

An important event was the start of integration of the Barrel Cryostat, WBS 1.3.1, starting with the welding to install the feedthroughs. This became possible with the tentative acceptance by BNL and transfer of ownership to CERN, with an agreement with KHI to repair a small leak on the end flange piece. This is the second detector to be installed, after the Tile Calorimeter, and we have been particularly anxious to keep these items on schedule.

As the various large production lines for the mechanical detector elements start to give accurate estimates of completion dates, as illustrated in the Line of Balance charts in Section 11 of this report, attention continues to be directed to the status of the many radiation-hard electronics deliverables, the radiation-soft version having been completed long ago. The first system to attain production of radiation-hard electronics is WBS 1.1.2, the electronics for the readout of the Silicon Strips. This is the ABCD chip in the DMILL process. The first thirty-five production wafers were delivered by ATMEL in mid-August. Due to a decrease in the backlog of orders in the vendor, the delivery is proposed to be accelerated, a phenomenon found for several electronics vendors, accompanied by very good cooperation in many aspects of the work. The Collaboration is placing a priority on checking the devices delivered in a timely way.

The most demanding radiation-hard ASIC chip in many ways is the Pixel Readout, WBS 1.1.1.3, as illustrated by the fact that the solution being pursued, the Deep Submicron process at IBM, has been preceded by several alternatives that were found to be lacking technically, or became too expensive as the situation of the vendors evolved. The prototype of this process proved promising and the cost is very favorable. The work has been intense on the next, hopefully final, submission now expected in October.

Another chip set exposed to heavy radiation is that for the TRT readout, WBS 1.2.5.
The front end ASIC, ASDBLR, should be close to release for production, but a troublesome new noise problem is being studied. The Muon electronics, less exposed to radiation, is progressing toward production.

The Liquid Argon Front End Board is in a radiation environment and is a large complex piece of electronics with a large number of ASICs and other components. Good progress has been achieved on the numerous chips needed, including the demanding analog SCA that is now ready for production. The problem of the radiation-hard voltage regulators, needed in numbers of about twenty on each board, continues to be addressed. The European vendor who will supply them to all the LHC experiments at the budgeted cost (rather than the cost of commercial vendors, ten times higher) is making progress, now able to deliver those for positive voltage. Those for negative polarity are some months away, causing delay in the Front End Boards.

4. TECHNICAL PROGRESS - SUBSYSTEM MANGERS' SUMMARIES

1.1 Subsystem Manager's Summary — Murdock Gilchriese (Lawrence Berkeley Lab.)

1.1.1 Pixels

The production of disk sectors has been slowed to complete the qualification of carbon-carbon plates and aluminum tubes used in the fabrication. The cutting of the carbon-carbon plates by the vendor has been difficult and final cutting will be tried at LBNL. There have been problems laser welding the aluminum tubes and this is under analysis. The remainder of the pixel mechanics is proceeding about as planned.

Preproduction sensors from the second vendor will be delivered in September.

The submission of the first IBM chip set has been delayed by 2-3 weeks, into October. The additional delay is largely from the MCC chip (being done in Genoa) and optical ICs(OSU and Siegen).

The layout of the version 3.x flex hybrid had to be modified to match changes in the IBM IC pinouts, and submission for fabrication should occur late in September.

Dummy 8" wafers were sent to the bump bonding vendors.

1.1.2 Silicon Strips

The first production ABCD wafers (35) were delivered about two weeks late at the end of the month. Testing of these wafers will occur in September and the test procedures tuned for production.

Some of the final tooling for module assembly continues to be delayed to resolve interfaces with the support structure. This is out of our control and it's not yet clear when this will be resolved. In the meantime, we have diverted design effort from the pixel mechanics to complete the design and fabrication of all of the remaining fixtures that will be necessary for production. About three man-months of design effort will be required.

1.1.3 RODs

The schedule for completing the layout of the production-model RODs continues to slide and first boards are now expected in October. There have been difficulties with the software for autorouting but no fundamental problems.

1.2 Subsystem Manager's Summary — Harold Ogren (Indiana University)

1.2.3

Hampton University was in full production all month. They had sufficient straws in inventory, and were limited only by summer shifts of personnel, vacations etc. We have had almost continual discussions with CERN about guaranteeing a constant supply of straws from Dubna and PNPI. It appears that the next shipment will be sent on time and should arrive at least 2 weeks before it is required. The Russian sites are increasing production rates on the reinforcing, which would mean that we could be well ahead on deliveries in a few months. The parts deliveries from Hampton this month were almost twice that of last month, allowing both Duke and Indiana to build up some inventory.

There are however a few areas on parts production that could cause slowdowns- Shell production has kept ahead of other parts production for the past year, but is still too slow.

HV plate production has begun to improve. The machining of the thick plates for type 1 and type 2 has been completed and has been tested at Fermilab. Ten new Type 3 type plates have been machined and are now being tested at Fermilab. Initial indication is very promising.

Module assembly is proceeding well. At Indiana three type 1 modules were completed in August. Duke production was down to one type 2, due to a long alignment process for module 2.10, which seemed to show misalignment in one corner. This was finally fixed and construction continued. Duke has begun production of the first type 3 module.

The basic production steps from gluing, leak testing, and wire stringing are now better understood, and are equal to or less than the projected times.

1.25 Electronics

Design activities are centered around trying to understand the significant increase in noise measured in the ASDBLR00 (just returned) vs. the spice prediction (~3300 e ENC vs. ~2200 e). The observed noise levels are enough higher to be very worrisome, but are probably within the range of useable values (possibly implying a small gain tweak to the chamber). The focus at the moment is on the new input protection added on the latest submission.

1.3 Subsystem Manager's Summary Richard Stroynowski (Southern Methodist University)

The barrel cryostat arrived at CERN in July. The acceptance tests found a small leak in the chimney weld. This leak will be repaired in the near future. In order not delay the start of the feedthrough installation the cryostat was provisionally accepted by BNL and its ownership was transferred to CERN. The repair work will not interfere with FT installation.

Several FT units - both signal and high voltage - were shipped to CERN and the shipping procedure was verified. Signal FT production reached halfway point. The preparations for their installation are under way and appear to be on schedule. The installation of the first FT is scheduled for October.

The prototypes of the barrel pedestal, crate with the bus bars and base plane have been received and are undergoing final tests. Their production will start in October and is on schedule. The delivery of warm cables is also on schedule.

The production and delivery of the motherboard system is going well. Sets corresponding to 10 modules have been already sent to the module construction sites. A problem with the calibration resistor network was identified in July during the cold tests of completed and instrumented modules. Several networks of calibration resistors were damaged by sparking making calibration of the corresponding channels impossible. Sparking is usually due to the residual dirt remaining in the module and was not anticipated for the ATLAS LArg calorimeter. However, the design and procedures used in the construction cannot guarantee absolute cleanliness of the modules. Therefore, the BNL group designed a protection circuit to minimize the effect of sparking on the resistor network. The prototypes of this circuit have been produced and will be tested in the beam test module in September. If this solution will be adopted, the cost of the addition of the protection circuits to the motherboard system is estimated to be about $200,000. The decision will be made in October.

The work on FEB design continues with the emphasis on completion of the layout and on the reduction of the number of voltage regulators needed on the board. Radiation testing of various components continues on schedule. The prototype of the Taiwanese optical transmitter failed in the irradiation. This prototype did not use correct components and a new prototype will be available for acceptance tests in October. The production of preamplifiers and layer sum boards is progressing well.

The FCAL production is also progressing well. Substantial effort was devoted recently to the understanding of the production schedule. Due to the initial delay in the start of the plate machining, FCAL production has effectively no schedule float. Any request for additional shortening of the schedule will require additional technical and financial assistance. The question of the FCAL production schedule will be discussed with ATLAS LArg group in October.

1.4 Subsystem Manager's Summary **Lawrence Price (Argonne National Lab.)**

Submodule and module production continues well. Final drawings for the special, cut submodules are being drawn up and we expect to review these and approve them for construction in the October ATLAS Week. Documentation of the extensive design and engineering analysis associated with the design of the extended barrel support saddle has been completed in preparation for an engineering meeting to be held in September. A small number of issues have been identified and will discussed and hopefully resolved at this meeting. Module instrumentation at MSU may have to move to a new building in Spring 2002. Plans are being made for the least disruptive transition. PMT Step 1 testing is continuing well, with 5 1/2 batches of 250 tubes completed at Illinois and 2 at UTA. 73% of the 3-in-1 cards have been shipped to CERN. All Front End Motherboards have been received and production testing is in preparation. Assembly of the cryostat scintillator mechanics will begin when ATLAS TC has completed its review.

1.5 Subsystem Manager's Summary **Frank Taylor (MIT)**

August was a month of continued series 2 MDT chamber production, further design and testing of associated electronics, CSC parts procurement and chamber production setup at BNL, improvements of design of CSC electronics and of production of chamber alignment parts and initial system testing at the CERN H8 facility.

MDT base chamber production for the second series continued at each chamber site. By the end of August a total of 3 EIS1 base chambers were completed at the BMC, 5 EMS4 chambers at Michigan and 5 EMS2 chambers at Seattle. The production installation of gas and tube-end ground covers was started at Seattle and Michigan - Seattle completing 6 EML2 chambers (series 1) and Michigan also concentrating on series 1 chambers (EMS5). The BMC service installation effort focused developing techniques for the gas system installation at Brandeis (Wellenstein) and on setting up an expanded production space on the CEA floor that will improve the efficiency of Faraday cage and gas system installation. Parts production of all essential components for the Faraday cages and gas system was started and each chamber site is developing an inventory. In addition the delivery of endplugs, tubes, spacer frames and chamber alignment parts continued to be ahead of critical path.

Significant advances were made in testing the prototype MDT readout electronics during August. The Chamber Service Module (CSM), designed by Chapman and associates at Michigan, was made to operate essentially error-free at several locations both in the US and Europe. A very large sample of cosmic tracks has been accumulated by Ahlen et al. at the BMC cosmic test facility. Ahlen et al. have

demonstrated a very good chamber resolution and the group has been observing the operation of the chamber system for some length of time.

Simplifications of the mezzanine readout card construction were developed and the tendering of HV and signal hedgehog cards proceeded in Europe. The ASD01A chip (for mezzanine card) was tested and found to meet specification except for the adjustable deadtime that was found to be shorter than design. An evaluation of the consequence of this is underway.

The pace of Cathode Strip Chamber (CSC) picked up at BNL. Polychronakos and associates have parts on hand for the first 4 production chambers and are proceeding on the procurement of most of the critical components for the entire series production. The plan calls for finishing the first 4 production chambers by the end of this calendar year. The production plan has been delayed somewhat due to increased testing of the first chamber component quality needed to certify vendors.

On the CSC electronics front work continued on redesigning the Amplifier Shaper Module (ASM) to be more robust with a better production yield, smaller cross talk and improved overload recovery. The later property will be important for the CSC response to neutron background - now being re-assessed by Polychronakos et al. Programming of the Sparsifier Processing Unit (SPU) by Stoker and company at UC-Irvine moved forward. Programming of the FPGAs on the prototype ROD also proceeded forward.

Alignment system parts for MDT chamber production (in-plane and PMO) continued ahead of the critical path at Brandeis. A significant milestone was achieved in August by the production and testing of the first alignment bar at Freiburg - in collaboration with the Brandeis alignment group. The bar was calibrated at Freiburg and shipped to CERN for the H8 test.

The H8 tests continued at CERN. Accomplished during August were the mounting of several phantom chambers and the commissioning of alignment parts and the DAQ system. Several critical lessons are being digested concerning chamber installation and the stability of monitors. One of the more significant findings from the H8 experience is the visceral realization of how large even one sector (1/8) of the big wheel is.

The need for integration engineering continued to be acute and the shortfall of local engineering manpower in the US became more evident.

1.6 Subsystem Manager's Summary **Robert Blair (Argonne National Lab.)**

Progress is being made on both system implementation and on system instrumentation (i.e. assuring that benchmarking yields meaningful timing information). The Supervisor RoI Builder (SRB) prototype is progressing. The choice of Gigabit ethernet has been made as a physical link within the SRB and this may prove useful in other areas of the readout.

1.10 Technical Coordination **David Lissauer (Brookhaven National Laboratory)**

Technical Coordination Project Office Meeting:
A meeting of the ATLAS Project Office took place. The main item for discussion was the preparation of the agenda for the system reviews that will take place in October. In October there will be three (3) system reviews: Magnet, Liquid Argon (Forward and Hadronic) and Trigger DAQ.

A new item that is gaining attention is the database needed for ATLAS installation in order to satisfy the nuclear installation regulations. One of the problems is to better understand the specifications and to make a determination of what CERN expects from the experiments to follow.

Envelopes:
Slow progress on finalizing the envelopes is being made. We are nearer to finalizing the main envelopes in the Z direction. The envelope in R is next. New conflicts were found mainly between the big wheel and the existing Hall structures.

LHC/ATLAS Interface: A lot of effort is being made to try to understand the interface between the ATLAS experiment and the LHC machine. The ATLAS experiment does not have the capability to be adjusted relative to the machine. (None exists after the initial placement for the Barrel Toroid and the Barrel Muon system. The ability to adjust the Barrel calorimeter and Inner tracker at later stages is not ruled out but will be very difficult.) This means that the LHC beam will have to accommodate the ATLAS experiment and be able to move the interaction point, if and when, there are changes in the experiment location relative to the beam. This kind of change is expected due to ground movements. They can be as large as 1 mm per year. Interactions with the machine people increased our understanding of the machine's capability.

Shielding and Activation meeting: Progress has been made in finalizing the design of the Shielding Disc and the small wheel that carries the first layer of the forward muon chambers. There are still a few open optimization questions that need to be done before we can finalize the design. They include inner radius of the shield disc, the exact interface between the small wheel, and the hub, etc.

LHC Schedule and Magnets: The bids for the first stage magnet integration are in. The bids are being evaluated at present. The first news is that the three (3) bids (from the three companies) are again very close. The cost is higher than officially expected. CERN is now looking toward the second integration step of the Magnets at CERN.

Conclusions:
Slow progress is being made in the ATLAS experiment. The TC team is small – progress is being made but concern persists that lots of problems are being overlooked.

5. OPEN ITEMS BETWEEN DOE/NSF AND U.S. ATLAS

a) Financial: There is $1,901,000 of available funding residing in management reserve and $6,080,000 of undistributed budget pending approval and implementation of MOU documents. Table 7-2 contains the summary of FY01 funds distribution. There was $2,609,000 requested in additional funding allocations during August.

b) Schedule: None.

c) Technical: None.

6. SUMMARY ASSESSMENT AND FORECAST

1. Financial Status

A total of $96,288,000 (58.8%) was authorized, held in reserve or identified as undistributed budget of the $163.75M Total Project Cost Objective. The details of the overall project cost objective are presented in

Table 6-1 reproduced overleaf from the U.S. ATLAS Project Plan as approved on 3/18/98 and revised to include cost changes approved through BCP # 48 (BCP # 49 is pending approval)

The details of the reported costs and reported obligations are presented in the Table 7-1 in Section 7 of this report. In addition Table7-2 shows the cost breakdown by institution and funding source.

The relationship between budget authority/cost/obligations (including an estimate of other accrued costs and obligations) is presented in Figure 9-1 in Section 9 of this report.

The level 2 CSSR statistics are presented in section 10. Performance analysis is included for major subsystems in section 8 of this report.

2. Schedule Status

See details in Figure 11-1.

The overall schedule status report is found in section 11.

The milestone log from the PMP, including revised forecast dates, is reproduced as section 12.

3. Baseline Change Proposals

Forty nine BCPs were received through August 2001. Forty six BCP's were approved, two were withdrawn, and one is pending review.

Table 6-1 reflects cost changes through BCP # 48.

TABLE 6-1: SUMMARY COST ESTIMATE

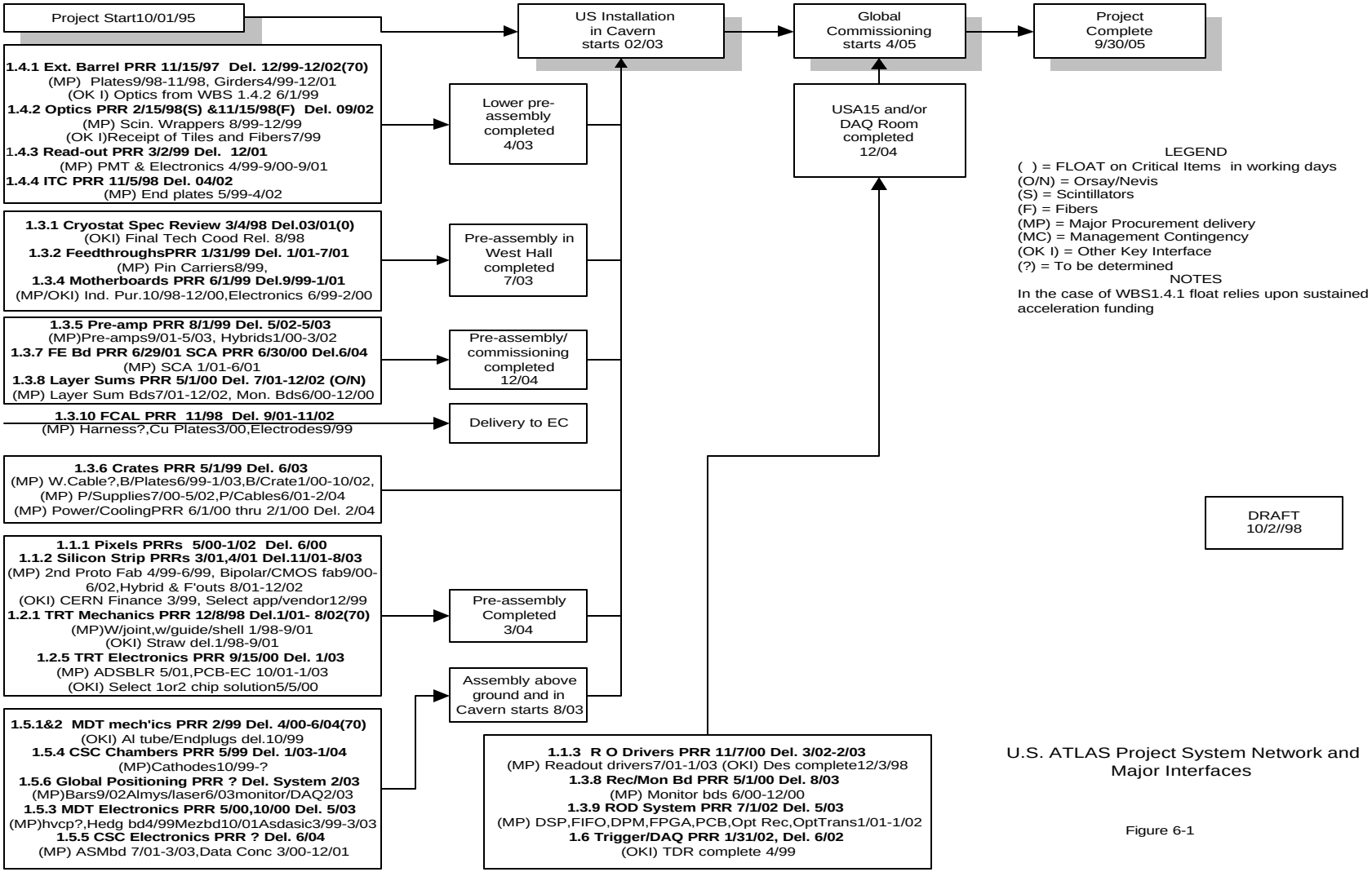
U.S.ATLAS Project
Summary Cost Estimate

Presented in (AY$ x 1000)

WBS No.	Description	Base Cost
	Technical Baseline	
1	U.S. ATLAS	
1.1	Silicon	17,795.3
1.2	TRT	9,194.0
1.3	LAr Calorimeter	43,771.7
1.4	Tile Calorimeter	9,148.2
1.5	Muon Spectrometer	26,391.2
1.7	Common Projects	9,179.1
1.8	Education	286.5
1.9	Project Management	8,279.0
1.10	Technical Coordination	450.0
	Subtotal	**124,495.0**
1.6	Trigger/DAQ Pre-Technical Baseline	3,117.9
	Subtotal	**3,117.9**
	Management Contingency	**8,851.7**
	Contingency	**19,446.0**
	Subtotal	**28,297.6**
	Technical Baseline	**155,910.5**
Items Outside of Approved Technical Baseline		
1.1.1	Pixels	-
1.6	Trigger/DAQ	**7,839.5**
	Subtotal	**7,839.5**
	Total Project Cost**	**163,750.0**

** Assumes funding profile of FY96=$1.7M, FY97=$3.7M, FY98=$10.05M,, FY99=$25.63 FY00=$28.4M, FY01=$26.8M, FY02=$21.9M, FY03=$25.9M,FY04=$14.7M, FY05=$5.0M.
project completion in 2005.
Includes cost changes for BCP 1-48. BCP 49 pending approval.

Figure 6-1 - Project System Network



U.S. ATLAS Project System Network and Major Interfaces

Figure 6-1

FUNDING

Table 7.1 - Summary of Funds Authorized & Total Costs and Commitments to Date

U.S. ATLAS Project
Summary of Funds Authorized
and
Total Costs and Commitments to Date
August 31, 2001
(AY$ x 1,000)

WBS No.	Description	Funds Authorized Thru FY01	Expenses + Commitments			Balance of Authorized Funds
			Expenses to Date	Open Commit	Total to Date	
1.1	Silicon	12,052	9,149	132	9,282	2,770
1.2	TRT	7,217	5,250	923	6,173	1,044
1.3	LAr Calorimeter	28,014	21,799	3,931	25,731	2,283
1.4	Tile Calorimeter	9,017	7,374	95	7,469	1,548
1.5	Muon Spectrometer	17,276	13,351	1,440	14,791	2,485
1.6	Trigger/DAQ	2,077	1,694	-	1,694	383
1.7	Common Projects	7,269	7,132	-	7,132	137
1.8	Education	49	47	-	47	2
1.9	Project Management	4,886	4,541	-	4,541	345
1.10	Technical Coordination	450	114		114	336
	Subtotal	88,307	70,452	6,522	76,974	11,333
	Management Reserve	1,901			-	1,901
	Contingency	-			-	-
	Subtotal	90,208	70,452	6,522	76,974	13,234
	Undistributed Budget	6,080			-	6,080
1	U.S. ATLAS Total AY$	96,288	70,452	6,522	76,974	19,314

Table 7.2 – FY01 Funds – U.S. ATLAS Summary by Institution and Subsystem

	Silicon			TRT			Liquid Argon			Tile			Muon			Trigger/DAQ			Common Projects			Education		Proj Mgtm			Tech Coord			U.S. ATLAS Total FY01			
	DOE		NSF	DOE		NSF	DOE		NSF	DOE		NSF	DOE		NSF	DOE		NSF	DOE		NSF	DOE	NSF	DOE		NSF	DOE		NSF	DOE		NSF	
Institution	Grant	Contract		Grant	Contract		Grant	Contract		Grant	Contract		Grant	Contract		Grant	Contract		Grant	Contract				Grant	Contract		Grant	Contract		Grant	Contract		Total
ANL	-		-	-		-	-		-		500		-		-		72		-	-	-	-	-	-		-	-		-	572	-	572
BNL	-		-	-		-		1,132	-					962					-	4,000	-	-	-	-	669		-	450		-	7,213	-	7,213
LBNL		1,775	-	-		-			-										-	-	-	-	-	-			-			-	1,775	-	1,775
SUNY/Albany	-		-	-		-			-										-	-	-	-	-	-			-			-	-	-	-
Arizona			-	-		-	299	153	-										-	-	-	-	-	-			-			299	153	-	451
Boston University			-	-		-			-				155						-	-	-	-	-	-			-			155	-	-	155
Brandeis University			-	-		-			-						731				-	-	-	-	-	-			-			-	-	731	731
UC Irvine			-	-		-			-				-		183			83	-	-	-	-	-	-			-			-	-	266	266
UC Santa Cruz			2,702	-		-			-										-	-	-	-	-	-			-			-	-	2,702	2,702
U of Chicago			-	-		-			-			723							-	-	-	-	-	-			-			-	-	723	723
Duke University			-	501					-										-	-	-	-	-	-			-			501	-	-	501
Hampton University			-			590			-										-	-	-	-	-	-			-			-	-	590	590
Harvard University			-						-						3,882				-	-	-	-	-	-			-			-	-	3,882	3,882
U of Illinois			-						-	76									-	-	-	-	-	-			-			76	-	-	76
Indiana University			-	-	616				-										-	-	-	-	-	-			-			-	616	-	616
MIT			-						-				190	239					-	-	-	-	-	-			-			190	239	-	429
Michigan State U			-						-			216						100	-	-	-	-	-	-			-			-	-	316	316
Nevis/Columbia			-						-										-	-	1,969	-	-	-		103	-		-	-	-	2,072	2,072
New Mexico	-	80	-						-										-	-	-	-	-	-		-	-		-	-	80	-	80
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U of Michigan			-						-				681						-	-	-	-	-	-		-	-		-	681	-	-	681
U of Oklahoma *			49						-										-	-	-	-	-	-		-	-		-	-	-	49	49
U of Pennsylvania			-	679					-										-	-	-	-	-	-		-	-		-	679	-	-	679
U of Pittsburg			-					50	201										-	-	-	-	-	-		-	-		-	-	50	201	251
U of Rochester			-						-										-	-	-	-	-	-		-	-		-	-	-	-	-
UT- Arlington			-						-			584							-	-	-	-	-	-		-	-		-	-	-	584	584
Southern Methodist U			-				67												-	-	-	-	-	-		-	-		-	67	-	-	67
SUNY/Stony Brook			-						426										-	-	-	-	-	-		-	-		-	-	-	426	426
Tufts University			-						-				-						-	-	-	-	-	-		-	-		-	-	-	-	-
U of Washington			-						-						1,377				-	-	-	-	-	-		-	-		-	1,377	-	1,377	1,377
U of Wisconsin	1,014		-						-							98			-	-	-	-	-	-		-	-		-	1,112	-	-	1,112
Total FY01	1,014	1,855	2,751	1,180	616	590	366	1,336	627	76	500	1,524	1,027	1,201	6,174	98	72	183	-	4,000	1,969	-	-	-	669	103	-	450	-	3,778	10,697	13,921	28,396
Reserve			-	-		-			-	-		-					-	-		-				139	199		-	-	-	139	199	337	
Contingency																									-	-		-	-	-	-	-	-	
Total FY01	1,014	1,855	2,751	1,180	616	590	366	1,336	627	76	500	1,524	1,027	1,201	6,174	98	72	183	-	4,000	1,969	-	-	-	808	302	-	450	-	3,778	10,697	14,120	28,734

* correction of prior month record of 436 to 49

8. PERFORMANCE ANALYSIS

Status through the month of August 2001 reflects the new baseline schedules for all subsystems. The re-baseline date was established on October 1, 2000 and the Estimate to Complete 01 (ETC 01) was defined as all tasks and resources required to complete the project. All prior efforts were equated to the actual costs expended. The schedules are resource loaded to the baseline funding of $163,750K with Contingency, Management Contingency, and Items Outside of the Approved Baseline shown on separate lines and excludes all NSF R&D funds.

The CSSR in section 10 shows $70,452.0k of the work has been performed, which represents approximately 56.6% of the work authorized to date. There is an unfavorable schedule variance of ($926.5k) or 1.3% behind the plan. There is a favorable cost variance of $891.3k or 1.2% under spent for the work accomplished. There are outstanding commitments of $6,522.2k at this time that do not show up in the performance. This analysis will provide a breakdown of these variances into the individual subsystems and identify the specific tasks that cause these variances.

WBS 1.1 Silicon

Summary

The CSSR shows that $9,219.5k of the work has been completed which represents 51.9% of the total effort for the Silicon subsystem. There is an unfavorable schedule variance of ($309.2k) or 3.2% behind the plan and a favorable cost variance of $70.1k or 0.8% under spent for the work accomplished. There are outstanding commitments of $132.4k at this time that do not show up in the performance.

Schedule Variance

The unfavorable schedule variance is concentrated in the following WBS level 3 elements:

WBS 1.1.2 Silicon Strip System SV = ($55.8k)

- Hybrids/Cables/Fanouts are behind plan ($19.0k)
- Module Assembly and Test is behind plan ($36.8k)

WBS 1.1.3 RODs SV = ($249.9k)

- Design ROD Cards is behind plan ($9.2k)
- ROD Test Stand is behind plan ($59.3k)
- ROD Prototypes is behind plan ($51.2k)
- ROD Prototype Evaluation is behind plan ($24.5k)
- ROD Production Model is behind plan ($101.3k)
- Purchase ROD Crates is behind plan ($4.2k)

Cost Variance

There is a favorable cost variance of $70.1k which is distributed as follows: Pixel ($202.2k), the Silicon Strip System $459.1k and the ROD Design and Fabrication ($186.7k).

WBS 1.2 TRT

Summary
The CSSR shows that $5,308.3k of the work has been completed which represents 57.7% of the total effort for the TRT subsystem. There is an unfavorable schedule variance of ($316.1k) or 5.6% behind the plan and a favorable cost variance of $58.0k or 1.1% under spent for the work accomplished. There are outstanding commitments of $923.0k at this time that do not show up in the performance.

Schedule Variance
The unfavorable schedule variance is concentrated in the following WBS level 3 elements

WBS 1.2.1 Barrel Mechanics SV = ($297.2k)

- Detector Elements are behind plan ($32.4k)
- Component Assembly is behind plan ($112.7k)
- Module Assembly #2 (Duke) is behind plan ($89.3k)
- Module Assembly #1 (IU) is behind plan ($60.1k)

WBS 1.3 LAr

Summary
The CSSR shows that $22,976.5k of the work has been completed which represents 54.5% of the total effort for the LAr subsystem. There is an unfavorable schedule variance of ($145.4k) or 0.6% behind the plan and a favorable cost variance of $1,177.1k or 5.1% under spent for the work accomplished. There are outstanding commitments of $3,931.4k at this time that do not show up in the performance.

Schedule Variance
The unfavorable schedule variance is concentrated in the following WBS level 3 elements:

1.3.2 Feedthroughs SV = ($32.9k)
1.3.3 Cryogenics SV = ($23.2k)
1.3.10 Forward Calorimeter SV = ($73.0k)

- FCAL1 Module Production and Tooling are behind plan ($22.5k)
- FCAL Electronics Design is behind plan ($33.8k)
- FCAL Production is behind plan ($16.6k)

Cost Variance
The favorable cost variance of $1,177.1k is a combination of positive and negative variances concentrated in the following WBS Level 3 elements.

- 131 Barrel Cryostat CV = $554.6k
- 132 Feedthroughs CV = ($123.6k)
- 133 Cryogenics CV = $667.1k
- 134 Readout Electrodes/MB CV = ($75.5k)
- 135 Preamp/Calibration CV = $138.9k
- 136 System Crate Integration CV = ($16.3k)
- 137 Front End Board CV = ($108.4k)
- 139 ROD System CV = $141.0k

WBS 1.4 Tile

Summary
The CSSR shows that $7,482.8k of the work has been completed which represents 81.8% of the total effort for the Tile subsystem. There is an unfavorable schedule variance of ($31.1k) or 0.4% behind the plan and a favorable cost variance of $109.0k or 1.5% under spent for the work accomplished. There are outstanding commitments of $95.2k at this time that do not show up in the performance.

Schedule Variance
The unfavorable schedule variance is concentrated in the following WBS level 3 elements:

1.4.4 Intermediate Tile Calorimeter SV = ($24.2k)

- Scintillator Preparation is behind plan ($17.4k)

Cost Variance
There is a favorable cost variance of $109.0k which is distributed as follows:

- 141 EB Mechanics $18.7k
- 142 EB Optics ($52.1k)
- 143 Readout $158.9k
- 144 ITC ($16.5k)

WBS 1.5 Muon

Summary
The CSSR shows that $12,930.40k of the work has been completed which represents 49.0% of the total effort for the Muon subsystem. There is an unfavorable schedule variance of ($80.5k) or 0.6% behind the plan and an unfavorable cost variance of ($420.6k) or 3.3% over spent for the work accomplished. There are outstanding commitments of $1,440.1k at this time that do not show up in the performance.

Schedule Variance
The unfavorable schedule variance is concentrated in the following WBS level 3 elements:

1.5.7 MDT Chambers SV = ($31.2k)

- Special Chamber Integration Drawings ($14.3k)
- Chamber Construction ($13.8k)

1.5.8 MDT Supports SV = ($38.4k)

- Chamber Mount Struts Design is behind plan ($15.2k)
- Integration with Support Structure Design is behind plan ($22.4k)

Cost Variance
The unfavorable cost variance of ($420.6k) is a combination of positive and negative variances concentrated in the following WBS Level 3 elements.

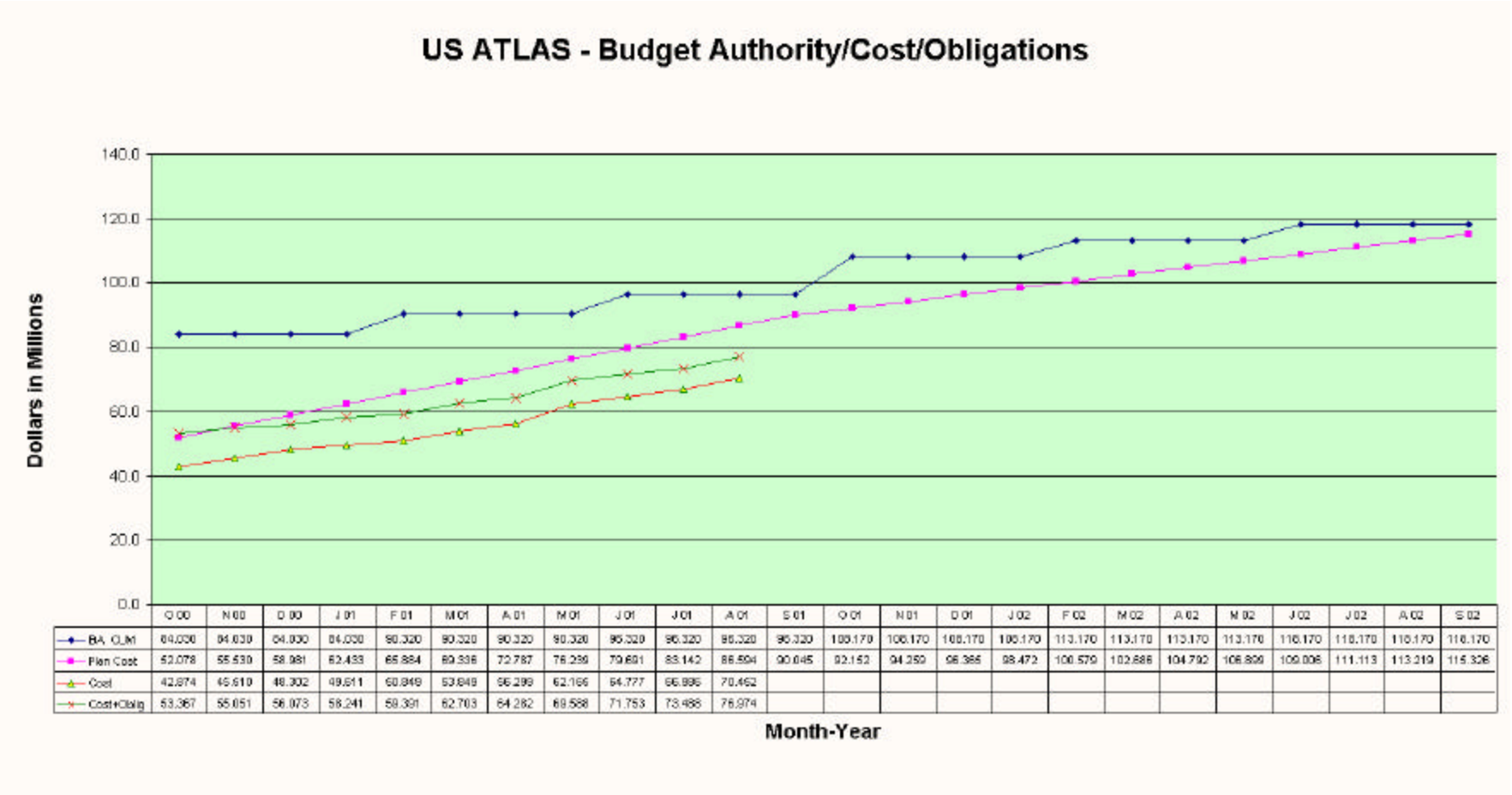
- 157 MDT Chambers CV = ($211.6k)
- 158 MDT Supports CV = ($41.6k)
- 159 MDT Electronics CV = $90.6k
- 1511 CSC Electronics CV = ($101.0k)
- 1512 Global Align System CV = ($157.0k)

WBS 1.6 Trigger/DAQ

Summary

The CSSR shows that $1,591.7k of the work has been completed which represents 51.1% of the total effort for the Trigger/DAQ subsystem. There is an unfavorable schedule variance of ($44.2k) or 2.7% behind the plan and an unfavorable cost variance of ($102.2k) or 6.4% over spent for the work accomplished. There are unfavorable cost variances of ($190.3k) for the Level 2 Supervisor, ($3.8k) for the Level 2 SCT Trigger and ($7.9k) for Architecture, but, these are offset by a favorable cost variance of 99.8k for the Level 2 Calorimeter Trigger. There are outstanding commitments of $0.1k at this time that do not show up in the performance.

9. BUDGET AUTHORITY COSTS AND OBLIGATIONS



	O 00	N 00	D 00	J 01	F 01	M 01	A 01	M 01	J 01	J 01	A 01	S 01	O 01	N 01	D 01	J 02	F 02	M 02	A 02	M 02	J 02	J 02	A 02	S 02
BA_OLM	84.030	84.030	84.030	84.030	90.320	90.320	90.320	90.320	96.320	96.320	96.320	96.320	108.170	108.170	108.170	108.170	113.170	113.170	113.170	113.170	118.170	118.170	118.170	118.170
Plan Cost	52.078	55.530	58.981	62.433	65.884	69.336	72.787	76.239	79.691	83.142	86.594	90.045	92.152	94.259	96.365	98.472	100.579	102.686	104.792	106.899	109.006	111.113	113.219	115.326
Cost	42.874	45.610	48.302	49.611	50.849	53.849	56.299	62.166	64.777	66.986	70.462													
Cost+Oblig	53.367	55.051	56.073	58.241	59.391	62.703	64.282	69.588	71.753	73.488	76.974													

10. WBS – COST SCHEDULE STATUS REPORT

Project Status Report
Section 10

U.S. ATLAS
Cost Schedule Status Report
Reporting Period Ending:08/31/01

		Cumulative To Date (k$)					At Completion (k$)			Complete (%)		
		Budgeted Cost		Actual Cost	Variance			Latest				
	WBS Element	Work Scheduled	Work Performed	Of Work Performed	Schedule	Cost	Budgeted AY $s	Revised Estimate	Variance	Scheduled	Performed	Actual
1.1	Silicon	9,528.7	9,219.5	9,149.3	(309.2)	70.1	17,795.3	17,795.3	-	53.5	51.8	51.4
1.2	TRT	5,624.4	5,308.3	5,250.3	(316.1)	58.0	9,194.0	9,194.0	-	61.2	57.7	57.1
1.3	Liquid Argon	23,121.9	22,976.5	21,799.5	(145.4)	1,177.1	43,771.7	43,771.7	-	52.8	52.5	49.8
1.4	TileCal	7,513.9	7,482.8	7,373.8	(31.1)	109.0	9,148.2	9,148.2	-	82.1	81.8	80.6
1.5	Muon	13,010.9	12,930.4	13,351.0	(80.5)	(420.6)	26,391.2	26,391.2	-	49.3	49.0	50.6
1.6	Trigger/DAQ	1,635.9	1,591.7	1,694.0	(44.2)	(102.2)	3,117.9	3,117.9	-	52.5	51.1	54.3
1.7	Common Projects [1]	7,132.2	7,132.2	7,132.2	-	-	9,179.1	9,179.1	-	77.7	77.7	77.7
1.8	Education [1]	47.2	47.2	47.2	-	-	286.5	286.5	-	16.5	16.5	16.5
1.9	Project Management [1]	4,541.0	4,541.0	4,541.0	-	-	8,279.0	8,279.0	-	54.8	54.8	54.8
1.10	Technical Coordination	113.7	113.7	113.7	-	-	450.0	450.0	-	25.3	25.3	25.3
Sub Total		72,269.8	71,343.3	70,452.0	(926.5)	891.3	127,612.9	127,612.9	-	56.6	55.9	55.2
Management Reserve							0.0	0.0	-			
Contingency							19,446.0	19,446.0	-			
Management Contingency							8,851.6	8,851.6	-			
Items Outside of Approved Baseline							7,839.5	7,839.5	-			
Escalation							0.0	0.0	-			
U.S. ATLAS Total		72,269.8	71,343.3	70,452.0	(926.5)	891.3	163,750.0	163,750.0	-	44.1	43.6	43.0

Notes: 1 LOE

FIGURE 11-1 - MILESTONE SCHEDULE STATUS REPORT

ID	Subsystem ID	Milestone	ETC 01 Baseline	Forecast	Actual
1		Project Start (10/1/95)	Sun 10/1/95	Sun 10/1/95	Sun 10/1/95
2	Tile L2/1	Start Submodule Procurement	Mon 9/1/97	Mon 9/1/97	Mon 9/1/97
3	Tile L2/2	Technology Choice for F/E Electronics	Sat 11/15/97	Sat 11/15/97	Sat 11/15/97
4	LAr L2/1	Cryostat Contract Award	Fri 7/24/98	Wed 8/5/98	Wed 8/5/98
5	LAr L2/2	Barrel FTs Final Design Review	Wed 9/30/98	Fri 10/2/98	Fri 10/2/98
6	TRT L2/1	Final Design Complete	Thu 12/31/98	Mon 12/7/98	Mon 12/7/98
7	LAr L2/4	FCAL Mech Design Complete	Mon 12/14/98	Wed 12/15/99	Wed 12/15/99
8	Tile L2/3	Start Module Construction	Sat 5/1/99	Mon 9/20/99	Mon 9/20/99
9	TDAQ L2/1	Select Final LVL2 Architecture	Fri 12/31/99	Fri 3/31/00	Fri 3/31/00
10	LAr L2/3	Start Elec.'s Production (Preamps)	Fri 6/30/00	Fri 6/30/00	Fri 6/30/00
11	Muon L2/1	Start MDT Chambers Lines 1 & 3	Mon 7/17/00	Fri 9/15/00	Fri 9/15/00
12	Muon L2/6	Kinematic Mount Design Complete	Tue 1/30/01	Tue 1/30/01	Tue 1/30/01
13	Tile L2/4	Start Production of MBs	Sun 4/1/01	Fri 3/30/01	Fri 3/30/01
14	LAr L2/9	Cryostat Arrives at CERN	Tue 5/15/01	Mon 7/2/01	Mon 7/2/01
15	TRT L2/4	Select Final Elec Design	Fri 6/15/01	Wed 8/30/00	Wed 8/30/00
16	Sil L2/1	Start Full Silicon Strip Elec Production	Fri 7/6/01	Sun 7/15/01	Sun 7/15/01
17	Sil L2/6	Pixels '1st IBM Prototype Submitted'	Thu 7/26/01	**Mon 10/8/01**	NA
18	Muon L2/2	Start CSC Chamber Production	Sat 9/1/01	Sat 9/1/01	NA
19	Sil L2/3	ROD Design Complete	Mon 10/1/01	Mon 10/1/01	NA
20	LAr L2/6	Level 1 Trigger Final Design Complete	Thu 10/4/01	**Tue 12/4/01**	NA
21	Muon L2/3	MDT Electronics ASD PRR	Fri 10/19/01	Fri 10/19/01	NA
22	Sil L2/2	Start Full Strip Module Production	Mon 1/7/02	Mon 1/7/02	NA
23	TRT L2/5	Start Production of ASICS	Fri 1/18/02	Fri 1/18/02	NA
24	LAr L2/10	Barrel FTs Production Complete	Fri 2/15/02	Fri 2/15/02	NA
25	Muon L2/4	Final Design of Global Align Devices	Mon 4/1/02	Mon 4/1/02	NA
26	Muon L2/5	CSC IC Production Complete	Wed 5/15/02	Wed 5/15/02	NA
27	LAr L2/8	MB System Production Complete	Sun 6/30/02	Sun 6/30/02	NA
28	TDAQ L2/3	LVL2 Trigger Prototype Complete	Mon 9/30/02	Mon 9/30/02	NA
29	Tile L2/6	Module Construction Complete	Mon 9/30/02	Mon 9/30/02	NA
30	Tile L2/5	All Elec.'s Components Delivered to ATLAS	Tue 10/1/02	Tue 10/1/02	NA
31	LAr L2/11	FCAL-C Delivered to EC	Thu 10/17/02	Thu 10/17/02	NA
32	Tile L2/7	All Modules Delivered to CERN	Mon 12/2/02	Mon 12/2/02	NA
33	LAr L2/7	ROD Final Design Complete	Thu 12/12/02	Thu 12/12/02	NA
34	TDAQ L2/2	LVL2 Trigger Design Complete	Tue 12/31/02	Tue 12/31/02	NA
35	TDAQ L2/4	Start Production	Wed 1/8/03	Wed 1/8/03	NA
36	TDAQ L2/5	Start Installation & Commissioning	Wed 3/5/03	Wed 3/5/03	NA
37	Muon L2/10	MDT Elec.'s Mezz Production Complete	Thu 3/6/03	Thu 3/6/03	NA
38	Sil L2/7	Pixels 'Start IBM Production'	Thu 3/13/03	Thu 3/13/03	NA
39	TRT L2/2	Module Production Complete (CUM 102)	Mon 3/31/03	Mon 3/31/03	NA
40	Sil L2/5	ROD Production/Testing Complete	Tue 6/24/03	Tue 6/24/03	NA
41	TRT L2/3	Barrel Construction Complete	Tue 9/16/03	Tue 9/16/03	NA
42	Sil L2/4	Compl Shipment of Silicon Strip Modules Prod	Mon 10/13/03	Mon 10/13/03	NA
43	Sil L2/8	Pixels 'Start IBM Outer Bare Module Prod'	Wed 10/22/03	Wed 10/22/03	NA
44	Muon L2/9	CSC ROD Production Complete	Wed 11/5/03	Wed 11/5/03	NA
45	LAr L2/12	FCAL-A Delivered to EC	Mon 12/8/03	Mon 12/8/03	NA
46	Muon L2/8	Kinematic Mount Production Complete	Mon 5/24/04	Mon 5/24/04	NA
47	Muon L2/7	MDT Chambers (U.S.) Prod Compl (Qty. 240)	Fri 8/27/04	Tue 9/14/04	NA
48	Muon L2/12	Global Align System Final Delivery	Thu 9/30/04	Thu 9/30/04	NA
49	Sil L2/9	Pixels 'Disk System at CERN'	Wed 10/13/04	Wed 10/13/04	NA
50	Muon L2/11	CSC Assembly/Test at CERN Complete	Fri 12/17/04	Fri 12/17/04	NA
51	TRT L2/6	Installation Complete	Tue 1/4/05	Tue 1/4/05	NA
52	TDAQ L2/6	Production Complete	Sat 7/30/05	Sat 7/30/05	NA
53	TDAQ L2/7	Installation & Commissioning Complete	Fri 9/30/05	Fri 9/30/05	NA

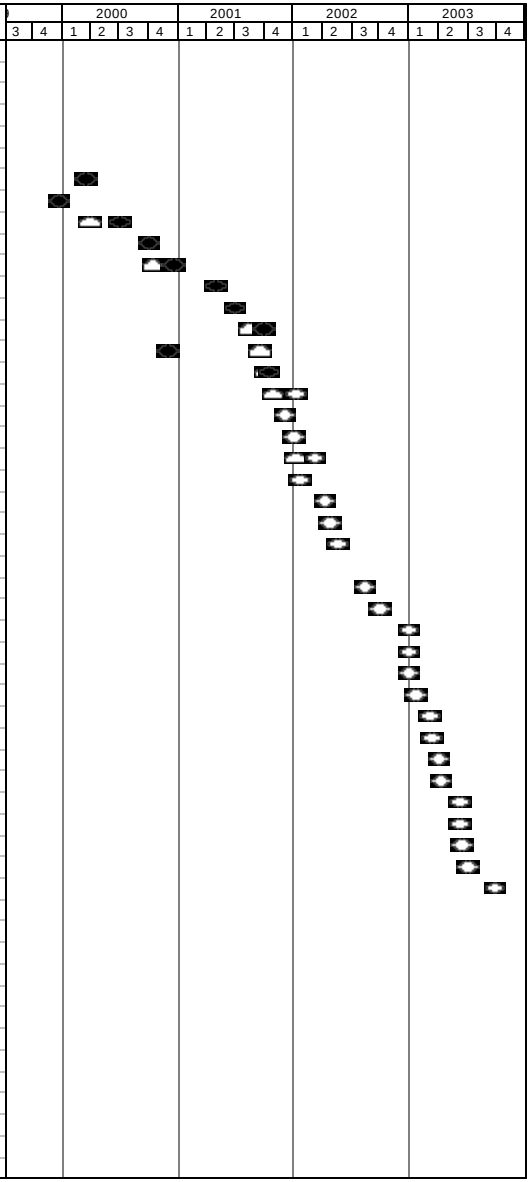
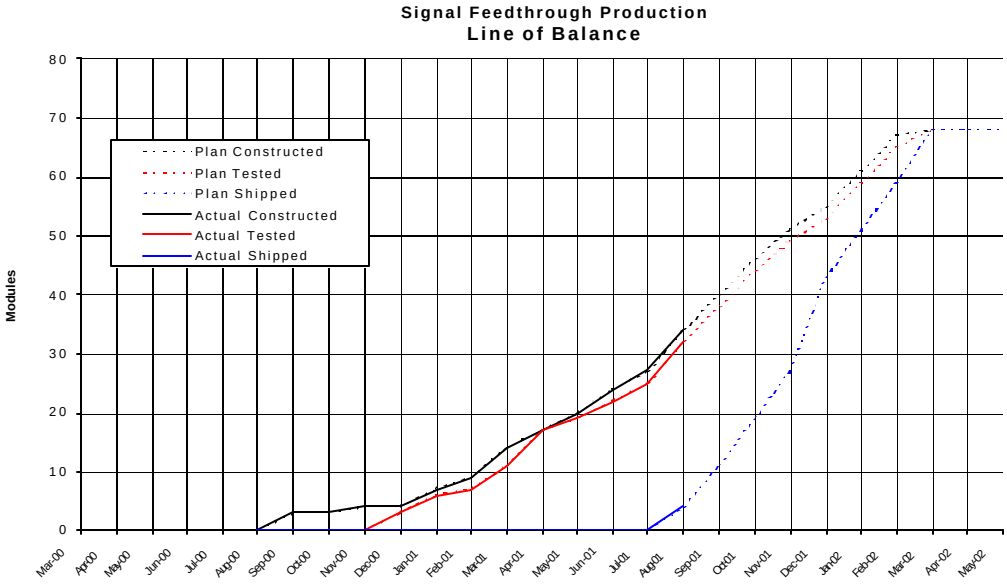
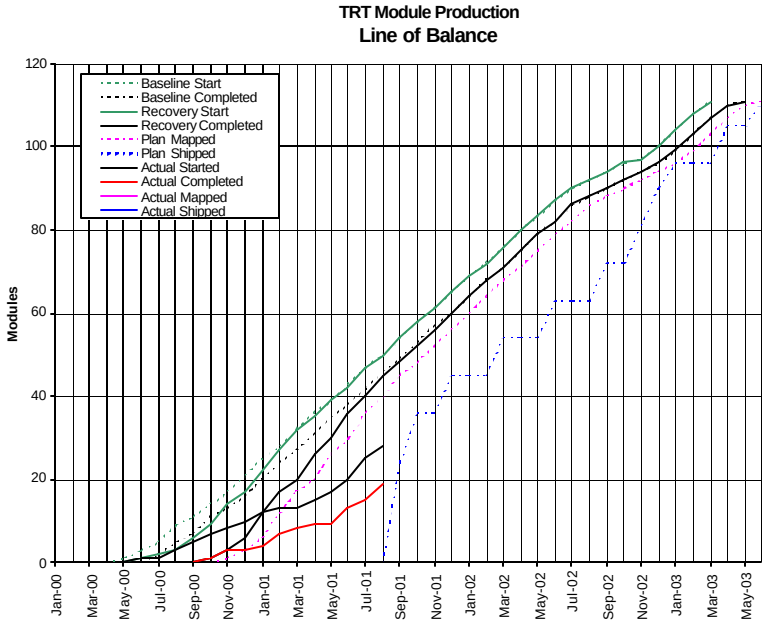


FIGURE 11-2

Figure 11-2 shows the Production status for the US ATLAS Project. You will note that the Signal Feedthrough Line of Balance has changed significantly since last month. The current Line of Balance reflects a rebaselining of the production, using the actual production to date, and a forecast production rate that can be reasonably achieved. The previous Line of Balance had not been changed since its inception over two years ago, and therefore did not reflect the problems encountered with pin carrier production. Since the problems with the pin carrier production appear to be resolved, it is now possible to develop and implement a credible production schedule.





12. MILESTONE LOG

The milestones have been updated with the new ETC 01 baseline dates.

U.S. ATLAS Major Project Milestones (Level 1)

Description	Baseline Schedule	Forecast (F) Date	Actual (A) Date
Project Start	01-Oct-95	01-Oct-95 (F)	01-Oct-95 (A)
Project Completion	30-Sep-05	30-Sep-05 (F)	

U.S. ATLAS Major Project Milestones (Level 2)

Subsystem	**Schedule Designator**	**Description**	**Baseline Schedule**	**Forecast (F) / Actual (A) Date**
Silicon (1.1)	SIL L2/1	Start Full Silicon Strip Electronics Production	06-Jul-01	15-Jul-01 (A)
	SIL L2/2	Start Full Strip Module Production	07-Jan-02	07-Jan-02 (F)
	SIL L2/3	ROD Design Complete	01-Oct-01	01-Oct-01 (F)
	SIL L2/4	Complete Shipment of Silicon Strip Module Production	13-Oct-03	13-Oct-03 (F)
	SIL L2/5	ROD Production/Testing Complete	24-Jun-03	24-Jun-03 (F)
	SIL L2/6	Pixels 1st IBM Prototype Submitted	26-Jul-01	**08-Oct-01 (F)**
	SIL L2/7	Pixels Start IBM Production	13-Mar-03	13-Mar-03 (F)
	SIL L2/8	Pixels Start IBM Outer Bare Module Prod	22-Oct-03	22-Oct-03 (F)
	SIL L2/9	Pixels Disk System at CERN	13-Oct-04	13-Oct-04 (F)
TRT (1.2) Mechanical	TRT L2/1	Final Design Complete	31-Dec-98	07-Dec-98 (A)
	TRT L2/2	Module Production Complete (CUM 102)	31-Mar-03	31-Mar-03 (F)
	TRT L2/3	Barrel Construction Complete	16-Sep-03	16-Sep-03 (F)
Electrical	TRT L2/4	Select Final Elec Design	15-Jun-01	30-Aug-00 (A)
	TRT L2/5	Start Production of ASICS	18-Jan-02	18-Jan-02 (F)
	TRT L2/6	Installation Complete	04-Jan-05	04-Jan-05 (F)
LAr Cal (1.3)	LAr L2/1	Cryostat Contract Award	24-Jul-98	05-Aug-98 (A)
	LAr L2/2	Barrel Feedthroughs Final Design Review	30-Sep-98	02-Oct-98 (A)
	LAr L2/3	Start Electronics Production (Preamps)	30-Jun-00	30-Jun-00 (A)
	LAr L2/4	FCAL Mechanical Design Complete	14-Dec-98	15-Dec-99 (A)
	LAr L2/6	Level 1 Trigger Final Design Complete	04-Oct-01	**04-Dec-01 (F)**
	LAr L2/7	ROD Final Design Complete	12-Dec-02	12-Dec-02 (F)
	LAr L2/8	Motherboard System Production Complete	30-Jun-02	30-Jun-02 (F)
	LAr L2/9	Cryostat Arrives at CERN	15-May-01	02-Jul-01 (A)
	LAr L2/10	Barrel Feedthroughs Production Complete	15-Feb-02	15-Feb-02 (F)
	LAr L2/11	FCAL-C Delivered to EC	17-Oct-02	17-Oct-02 (F)
	LAr L2/12	FCAL-A Delivered to EC	08-Dec-03	08-Dec-03 (F)

U.S. ATLAS Major Project Milestones (Level 2) (Continued)

Subsystem	Schedule Designator	Description	Baseline Schedule	Forecast (F) / Actual (A) Date
Tile Cal (1.4)	Tile L2/1	Start Submodule Procurement	01-Sep-97	01-Sep-97 (A)
	Tile L2/2	Technology Choice for F/E Electronics	15-Nov-97	15-Nov-97 (A)
	Tile L2/3	Start Module Construction	01-May-99	20-Sep-99 (A)
	Tile L2/4	Start Production of Motherboards	01-Apr-01	30-Mar-01 (A)
	Tile L2/5	All Electronic Components Delivered to CERN	01-Oct-02	01-Oct-02 (F)
	Tile L2/6	Module Construction Complete	30-Sept-02	30-Sep-02 (F)
	Tile L2/7	All Modules Delivered to CERN	02-Dec-02	02-Dec-02 (F)
Muon (1.5)	Muon L2/1	Start MDT Chambers Lines 1 and 3	17-Jul-00	15-Sep-00 (A)
	Muon L2/2	Start CSC Chamber Production	01-Sep-01	01-Sep-01 (F)
	Muon L2/3	MDT Electronics ASD PRR	19-Oct-01	01-Oct-01 (F)
	Muon L2/4	Final Design of Global Alignment Devices Complete	01-Apr-02	01-Apr-02 (F)
	Muon L2/5	CSC IC Production Complete	15-May-02	15-May-02 (F)
	Muon L2/6	Kinematic Mount Design Complete	30-Jan-01	30-Jan-01 (A)
	Muon L2/7	MDT Chambers (U.S.) Production Complete	27-Aug-04	14-Sep-04 (F)
	Muon L2/8	Kinematic Mount Production Complete	24-May-04	24-May-04 (F)
	Muon L2/9	CSC ROD Production Complete	05-Nov-03	05-Nov-03 (F)
	Muon L2/10	MDT Elec.'s Mezzanine Production Complete	06-Mar-03	06-Mar-03 (F)
	Muon L2/11	CSC Assembly/Testing at CERN Complete	17-Dec-04	17-Dec-04 (F)
	Muon L2/12	Global Alignment System Final Delivery	30-Sep-04	30-Sep-04 (F)
Trigger/ DAQ (1.6)	TDAQ L2/1	Select Final LVL2 Architecture	31-Dec-99	31-Mar-00 (A)
	TDAQ L2/2	LVL2 Trigger Design Complete	31-Dec-02	31-Dec-02 (F)
	TDAQ L2/3	LVL2 Trigger Prototype Complete	30-Sep-02	30-Sep-02 (F)
	TDAQ L2/4	Start Production	08-Jan-03	08-Jan-03 (F)
	TDAQ L2/5	Start Installation & Commissioning	05-Mar-03	05-Mar-03 (F)
	TDAQ L2/6	Production Complete	30-Jul-05	30-Jul-05 (F)
	TDAQ L2/7	LVL2 Installation & Commissioning Complete	30-Sep-05	30-Sep-05 (F)

U.S. ATLAS Major Project Milestones (Level 4)

WBS	Schedule Designator	U.S. ATLAS Responsibility Completion Description	ETC01 Baseline Scope Planned Completion Date	Forecast (F)/ Actual (A) Baseline Scope Completion Date	ATLAS Required Date	Baseline Scope Planned Float (Months)
Silicon						
1.1.2	Sil L4/1	Complete Shipping of Silicon Strip Prod Modules	10/03	10/03	4/03	-6
1.1.3	Sil L4/2	RODs 45% Production Complete	9/02	9/02	6/03	9
1.1.1	Sil L4/3	Pixels 'Disk System at CERN'	10/04	10/04	12/04	2
TRT						
1.2.1	TRT L4/1	Barrel Modules Ship to CERN Complete	8/02	8/02	3/03	7
1.2.5	TRT L4/2	ASDBLRs Ship to LUND Complete	10/02	10/02	11/02	1
	TRT L4/3	ASDBLRs Ship to CERN Complete	11/02	11/02	12/02	1
	TRT L4/4	PCB-Endcaps Ship to CERN Complete	4/03	4/03	10/03	6
LAr						
1.3.1	LAr L4/1	Cryostat Final Acceptance Test Complete	8/01	**8/01 (A)**	11/01	3
1.3.2	LAr L4/2	Signal FT Installation Complete	11/02	11/02	10/02	-1
	LAr L4/3	HV FT End-Cap C Install Complete	2/02	2/02	11/01	-3
	LAr L4/4	HV FT Barrel Install Complete	11/01	11/01	5/02	6
	LAr L4/5	HV FT End-Cap A Install Complete	12/02	12/02	9/02	-3
1.3.3	LAr L4/6	LAr Cryogenics Vendor Install Complete	9/03	9/03	12/03	3
1.3.4.1	LAr L4/7	Last Del of Readout Electrodes	12/02	12/02	10/02	-2
1.3.4.2	LAr L4/8	MBs Ship to Annecy,Saclay (France)	6/02	6/02	9/02	3
1.3.5.1	LAr L4/9	Preamp Deliveries to FEB Complete	5/03	5/03	3/04	10
1.3.5.2	LAr L4/10	Prec Calor Calib Production Complete	N/A	N/A	N/A	N/A

U.S. ATLAS Major Project Milestones (Level 4) (Continued)

WBS	Schedule Designator	U.S. ATLAS Responsibility Completion Description	ETC01 Baseline Scope Planned Completion Date	Forecast (F)/ Actual (A) Baseline Scope Completion Date	ATLAS Required Date	Baseline Scope Planned Float (Months)
Lar (Continued)						
1.3.6.1	LAr L4/12	Pedestal Ship to CERN Complete	12/01	12/01	7/02	7
	LAr L4/13	Barrel Ship to CERN Complete	12/01	12/01	3/03	15
1.3.6.2	LAr L4/14	Cables Shipping Complete	10/02	10/02	3/03	5
	LAr L4/15	Baseplane Last Delivery to CERN Complete	10/02	10/02	3/03	5
1.3.6.3	LAr L4/16	EC Crates Last Delivery to CERN Complete	10/02	10/02	3/03	5
	LAr L4/17	Barrel Crates Last Delivery to CERN Complete	10/02	10/02	3/03	5
1.3.6.4	LAr L4/18	Controls Ship to CERN Complete	9/03	9/03	5/04	8
	LAr L4/19	Power Supplies Last Delivery Complete	9/04	9/04	5/04	-4
1.3.6.5	LAr L4/21	Thermal Contacts (Proto) Last Delivery Complete	9/02	9/02	9/02	0
1.3.7.1	LAr L4/22	FEB Last Delivery Complete	8/04	8/04	1/05	5
1.3.7.4	LAr L4/24	Last Driver Delivery to FEB Complete	4/04	4/04	5/04	1
1.3.8.1	LAr L4/26	Layer Sums Last Delivery to FEB Complete	12/02	12/02	3/04	15
1.3.8.2	LAr L4/27	I/F to Level 1 Ship to CERN Complete	8/04	8/04	12/04	4
1.3.9	LAr L4/28	ROD System Final Prototype Complete	8/02	8/02	8/02	0
1.3.10	LAr L4/29	Deliver Finished FCAL-C to EC	10/02	10/02	10/02	0
	LAr L4/30	Deliver Finished FCAL-A to EC	12/03	12/03	11/03	-1
	LAr L4/31	FCAL Elec.'s Summ Bds Ready for Installation	12/01	12/01	2/02	2
	LAr L4/32	FCAL Elec.'s Cold Cables Testing Complete	11/01	11/01	2/02	3

U.S. ATLAS Major Project Milestones (Level 4) (Continued)

WBS	Schedule Designator	U.S. ATLAS Responsibility Completion Description	ETC01 Baseline Scope Planned Completion Date	Forecast (F)/ Actual (A) Baseline Scope Completion Date	ATLAS Required Date	Baseline Scope Planned Float (Months)
Tile						
1.4.1	Tile L4/1	Submodules Construction Compl (Original Baseline Scope –Qty. 45)	7/01	3/01 (A)	8/01	5
	Tile L4/2	EB Module Ship to CERN Complete (Qty. 40)	12/01	12/01	7/02	7
1.4.2	Tile L4/3	Optics Instrumentation at ANL & MSU Complete	9/02	9/02	11/02	2
1.4.3	Tile L4/4	PMT Ship to ATLAS Complete	1/02	1/02	7/02	6
1.4.3	Tile L4/5	Readout Ship to ATLAS Complete	**11/02**	**11/02**	**3/03**	**4**
1.4.4	Tile L4/6	Gap Submodules Ship to ANL & BCN Compl (Original Baseline Scope-Qty. 77)	7/01	4/01 (A)	8/01	4
1.4.1	**Tile L4/7**	**Submodule Construction Compl (Qty. 576)**	**3/02**	**3/02**	**7/02**	**4**
1.4.1	**Tile L4/8**	**EB Module Ship to CERN Complete (Qty. 64)**	**12/02**	**12/02**	**1/03**	**1**
1.4.4	**Tile L4/9**	**Gap Submodules Ship to ANL & BCN Compl (Qty. 128)**	**7/02**	**7/02**	**7/02**	**0**

Muon						
1.5.7 (1)	Muon L4/1	MDT Chamber Prod Complete (BMC Qty. 80)	6/04	6/04	2/04	-4
		MDT Chamber Prod Complete (Mich Qty. 80)	8/04	8/04	2/04	-6
		MDT Chamber Prod Complete (Seattle Qty. 80)	8/04	8/04	2/04	-6
1.5.8 (2)	Muon L4/2	MDT Mounts Prod Complete/Delivered to Chambers	10/03	10/03	2/04	4
1.5.9 (3)	Muon L4/3	MDT Elec.'s Mezzanine Bd Production Complete	3/03	3/03	2/03	-1
	Muon L4/4	MDT Elec.'s Hedgehog Production Complete	12/01	12/01	4/01	-8
1.5.4	Muon L4/5	CSC Chambers Production Complete	1/03	1/03	4/04	15
1.5.11 (5)	Muon L4/6	ASMs Production Complete	4/04	4/04	4/04	0
	Muon L4/7	Sparsifiers Ship to CERN	3/04	3/04	10/04	7
	Muon L4/8	RODs Ship to CERN	3/04	3/04	10/04	7
	Muon L4/9	Support Electronics Ship to CERN	3/04	3/04	10/04	7
1.5.12 (6)	Muon L4/10	Align Bars Ship to CERN	3/04	3/04	12/04	9
	Muon L4/11	Proximity Monitors Ship to CERN	12/03	12/03	12/04	12
	Muon L4/12	Multi-Point System Ship to CERN	3/03	3/03	3/05	24
	Muon L4/13	DAQ Ship to CERN	9/04	9/04	12/04	3
Trig/DAQ						

13. NSF COST SCHEDULE STATUS REPORT

Fourteen US ATLAS institutions will receive funding under the NSF Cooperative Agreement (No. PHY 9722537) in FY01. Technical progress reports are given in the respective subsystem paragraphs of Section 4. The NSF Cost Schedule Status Report (CSSR) in this section covers these 14 institutions, in addition to the Education, Institutional Dues and Common Project items which will be funded by the NSF, and also the Items Outside Approved Baseline and Contingency.

Status through the month of August 2001 reflects the new baseline schedules for all subsystems. The schedules are resource-loaded to the baseline funding of $163,750K with Contingency, Management Contingency and Items Outside of the Approved Baseline shown on separate lines, excluding all NSF R&D funds. The anticipated NSF contribution to the baseline funding is $60,800K

We note that more than half of the universities in the NSF CSSR are, or have been, funded by both NSF and DOE, while we manage the project without distinguishing the agency source of funding. For this reason, the NSF+DOE Budgeted AY$s column in Table 13-1 includes all Project funds allocated to each institution, while the last two columns to the far right show the contribution of each agency.

The re-baseline date was established as October 1 2000 and the FY 01 Estimate to Complete (ETC-01) was defined as all tasks and resources required too complete the project. These tasks were scheduled and the necessary resources were loaded into the schedules. All prior efforts were equated to the actual cost expended. There was a negative schedule variance along with a positive cost variance in the old baseline and this resulted in a reduction in both the work scheduled and the work performed in the new baseline.

The CSSR shows that $24,515.6K of the work has been completed which represents approximately 43.0% of the work authorized to date. There is an unfavorable schedule variance of $627.3 or 2.5% behind the plan and a favorable cost variance of $14.8K or 0.1% under spent for the work accomplished. There are outstanding commitments of $885.0k at this time that do not show up in the performance.

Schedule Variance

Hampton – SV = ($112.7k)

WBS 1.2.1.1.3 Barrel Module Component Assembly is behind plan $112.7k

University of Texas at Arlington – SV = ($298.9k)

WBS 1.4.4.1.3 Procurement effort for the Gap Sub-module Production is behind plan $298.9k

Cost Variance

Although the overall cost variance for NSF Institutions is an unfavorable $14.8k it is comprised of both positive and negative variances as follows:

- Brandeis – CV = ($181.0k)
  - Over spent on tooling ($59.3k)
  - Charging against Global System Production tasks ($136.2k)
  - These are offset by positive cost variances for 1.5.7.7 and 1.5.12.1
- Harvard – CV = ($416.8k)
  - Over spent on Common Procurements ($327.2k)
  - Chamber Fabrication and Construction ($53.5k)
  - MDT Supports ($26.9k)
- Nevis – CV = ($100.5K)
  - Over spent on the FEB ($123.6k)
  - Offset by small positive CV in the ROD System and Beam Tests
- MSU CV = ($78.7K)
  - Over spent on Extended Barrel Optics ($28.4k)
  - Over spent on Trigger/DAQ ($59.2k)
- UCSC CV = $129.7k
  - Under spent in the area of Design, Development and Prototypes
- University of Rochester CV = $662.6K
  - Under spent by $343.7k on Vendor Manufacturing but shows an outstanding commitment of $317.8k
  - Under spent by $219.7k on Manufacturing Monitoring
- University of Chicago CV = $140.2K
  - Under spent by $145.7k on Readout
  - Over spent by ($14.5k) Extended Barrel Module
- University of Washington CV = ($105.7k)
  - Over spent in the Common Procurement of the Gas Supply and Spacer Frame

Table 13

Cost Schedule Status Report

Reporting Period Ending:8/31/01

	Cumulative To Date (k$)					At Completion (k$)			Complete (%)			Budgeted AY $s	
	Budgeted Cost		Actual Cost	Variance		NSF + DOE	Latest						
Institution	Work Scheduled	Work Performed	Of Work Performed	Schedule	Cost	Budgeted AY $s	Revised Estimate	Variance	Scheduled	Performed	Actual	NSF	DOE
Brandeis	1,868.7	1,865.1	2,046.1	(3.6)	(181.0)	2,848.5	2,848.5	-	65.6	65.5	71.8	2,413.3	435.2
Harvard	2,899.6	2,858.2	3,275.0	(41.4)	(416.8)	6,909.4	6,909.4	-	42.0	41.4	47.4	6,909.4	
Columbia Nevis Lab [2]	3,555.4	3,547.9	3,648.4	(7.5)	(100.5)	9,458.1	9,458.1	-	37.6	37.5	38.6	9,196.8	261.3
Hampton University	1,105.1	992.4	937.1	(112.7)	55.3	1,495.3	1,495.3	-	73.9	66.4	62.7	1,495.3	
Michigan State University	630.4	586.5	665.2	(43.9)	(78.7)	1,075.5	1,075.5	-	58.6	54.5	61.9	1,040.2	35.3
Oklahoma	134.8	134.5	142.6	(0.3)	(8.1)	393.7	393.7	-	34.2	34.2	36.2	342.3	51.4
Pittsburg	529.9	526.7	560.4	(3.2)	(33.7)	2,033.6	2,033.6	-	26.1	25.9	27.6	1,920.1	113.5
SUNY Stony Brook	500.1	492.1	505.0	(8.0)	(12.9)	1,089.1	1,089.1	-	45.9	45.2	46.4	1,083.9	5.2
University of California Irvine	658.7	604.7	607.1	(54.0)	(2.4)	2,010.4	2,010.4	-	32.8	30.1	30.2	1,715.8	294.6
University of California Santa Cruz	3,413.9	3,406.1	3,276.4	(7.8)	129.7	3,984.5	3,984.5	-	85.7	85.5	82.2	3,286.3	698.2
University of Rochester	5,106.1	5,099.5	4,436.9	(6.6)	662.6	9,287.6	9,287.6	-	55.0	54.9	47.8	8,936.7	350.9
University of Texas Arlington	1,338.9	1,040.0	1,073.2	(298.9)	(33.2)	1,534.7	1,534.7	-	87.2	67.8	69.9	1,431.0	103.7
University of Chicago	2,069.1	2,064.3	1,924.1	(4.8)	140.2	2,126.9	2,126.9	-	97.3	97.1	90.5	2,115.4	11.5
Washington	1,332.2	1,297.6	1,403.3	(34.6)	(105.7)	3,241.0	3,241.0	-	41.1	40.0	43.3	3,241.0	
Education [3]				-	-	286.5	286.5	-	-	-	-	286.5	
Institutional Dues [3]				-	-	2,036.6	2,036.6	-	-	-	-	1,930.4	106.2
Common Projects [3]				-	-	7,142.5	7,142.5	-	-	-	-	652.2	6,490.3
Sub Total	25,142.9	24,515.6	24,500.8	(627.3)	14.8	56,953.9	56,953.9	-	44.1	43.0	43.0	47,996.6	
								-				-	
Items outside baseline						2,388.5	2,388.5	-				2,388.5	
Management Contingency						4,921.7	4,921.7	-				4,921.7	
Contingency						4,219.9	4,219.9	-				4,219.9	
Project Management						1,273.3	1,273.3	-				1,273.3	
Total (with DOE Funds included)	25,142.9	24,515.6	24,500.8	(627.3)	14.8	69,757.3	69,757.3	-	36.0	35.1	35.1		8,957.3
Total NSF Funds												60,800.0	
Note 1. Not used												60,800.0	69,757.30
2. Nevis Costs do not currently include Project management costs												-	
3. Treated as LOE based on actuals reported													

14. DETAILED TECHNICAL PROGRESS

1.1 SILICON

Milestones with changed forecast dates:

1.1.1.3.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
1st IBM prototype submitted (FE-I1)	26-Jul-01	17-Sep-01	8-Oct-01	Delayed (See #1)
FE-D3 wafers arrive	22-Aug-01	22-Aug-01	22-Dec-01	Delayed (See #2)
1st IBM prototype delivered	24-Oct-01	12-Nov-01	7-Dec-01	Delayed (See #3)
Complete initial wafer probe FE-I1	7-Nov-01	26-Nov-01	21-Dec-01	Delayed (See #4)
First bump bonded FE-I1 assemblies arrive	9-Jan-02	9-Jan-02	15-Feb-02	Delayed (See #5)

Note #1-2, 4 Testing of the Analog Test chip has revealed large threshold dispersion. This must be improved before full submission. Other accumulated delays suggest a total ten-week delay in the submission date.
Note #3 See note #2 above. Note that due to reduced foundry demand, the turnaround for IBM has been observed to be as low as 5 weeks, so the 8-week processing time assumed here should be reasonable.
Note #5 See Note#2 above. We are assuming a 6-week turnaround for the bump-bonding vendor. Significant processing of dummy wafers will be performed first to validate the processing of 8" wafers

1.1.1.4.1 Design

Milestone	Baseline	Previous	Forecast	Status
Optical FDR	31-Jan-02	31-Jan-02	15-Feb-02	Delayed (See #1)

Note #1 Synchronized with pixel week in February.

1.1.2.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
First Lots Delivered	23-Nov-01	23-Nov-01	27-Aug-01	Completed

1.1.2.3.1 Design of Assembly & Test Tooling

Milestone	Baseline	Previous	Forecast	Status
Module PRR	3-Sep-01	3-Sep-01	1-Feb-02	Delayed (See #1)
Compl Design of Preprod Mod Assy/Test	3-Sep-01	3-Sep-01	3-Oct-01	Delayed (See #2)

Note #1 Given the delay discussed in #1 above this is the current expected date for the US module assembly PRR.
Note #2 The pre-prod series awaits a resolution of the module fixation point problem. The design of the fixation point is a UK responsibility and we are dependant on that.

1.1.2.3.3 Production

Milestone	Baseline	Previous	Forecast	Status
Complete Preproduction Module Assembly	30-Jul-01	30-Oct-01	30-Nov-01	Delayed (See #1)
Complete Preproduction Module Testing	3-Sep-01	30-Oct-01	15-Nov-01	Delayed (See #2)
Start Full Strip Module Production	7-Jan-02	7-Jan-02	1-Feb-02	Delayed (See #3)

Note #1-2 Require pre-production hybrids which won't be available until the end of summer. requires resolution of module fixation point design.
Note #3 Defined as date of module assembly PRR.

1.1.3.4.3 SCT/Pixel Test Stand Software

Milestone	Baseline	Previous	Forecast	Status
Production Diagnostic Test Stand Completed	29-Sep-00	29-Aug-01	29-Oct-01	Delayed (See #1)

Note #1 The test stand software is completely functional for the production testing. This software will be updated for more efficiency in the next few months. The remaining testing is of the hardware (fabricated) to loop back the outputs to the FIFOs at the input to the ROD. The loop back cards are used to verify the output data quality. These loop back cards will be tested when more RODs are fabricated. Jan Valenta will arrive at LBL from Academy of Sciences of the Czech Republic in late September to complete the work of Lukas Tomasek. Lukas will continue to support the effort from the Czech Republic till October and train Jan. No schedule impacts are forecasted.

1.1.3.7.1 Updating of ROD to Production Model

Milestone	Baseline	Previous	Forecast	Status
SCT ATLAS ROD PRR	1-Oct-01	15-Apr-02	15-Nov-02	Delayed (See #1)

Note #1 The PRR is contingent on completion of the user evaluation. Please see 1.1.3.6.3 SCT ROD user evaluation complete for details.

1.1.3.7.3 Evaluation of Production Model

Milestone	Baseline	Previous	Forecast	Status
Release Production Dwg/Specs	16-May-01	15-Aug-01	10-Sep-01	Delayed (See #1)
Release Production Bids	4-Jul-01	20-Aug-01	20-Sep-01	Delayed (See #2)
Bid Evaluation Complete	15-Aug-01	7-Sep-01	15-Sep-01	Delayed (See #3)

Note #1 The current progress show that the drawing will not be ready till 10 September of 2001. This was caused by the extended time required to debug the proto ROD. Production is not expected to slip past the macro assembly site need date.
Note #2 The first bid to be released is for the Production model and 5% production of PC cards (25 ea.). The large production bid will not be released till the user evaluation at CERN system test is complete. These card are needed for the system test at CERN and evaluation of the ROD at the macro assembly sites.
Note #3 The delay will have no impact on needs.

1.1.3.8.2 SCT ROD Production

Milestone	Baseline	Previous	Forecast	Status
ROD 45% Production complete	16-Jan-02	16-Jan-02	16-Jul-02	Delayed (See #1)

Note #1 The production can not start till ATLAS has significant user evaluation and a review of the SCT Off-detector Electronics.

1.1.1 Pixels — Murdock Gilchriese (Lawrence Berkeley Lab.)

1.1.1.1 Mechanics

The production of disk sectors has been slowed to complete the qualification of carbon-carbon plates and aluminum tubes used in the fabrication. The cutting of the carbon-carbon plates by the vendor has been difficult and final cutting will be tried at LBNL. There have been problems laser welding the aluminum tubes and this is under analysis. The remainder of the pixel mechanics is proceeding about as planned.

1.1.1.2 Sensors

Preproduction sensors from the second vendor will be delivered in September. Discussion regarding the release of management contingency for production should begin in October.

1.1.1.3 Electronics

The submission of the first IBM chip set has been delayed by 2-3 weeks, into October. The additional delay is largely from the MCC chip (being done in Genoa) and optical ICs(OSU and Siegen). Irradiation of IBM test structures and the prototype analog chip should occur in September. The rate of progress on the test system has increased some, but is still limited by competition for manpower with the RODs.

1.1.1.4 Hybrids

The layout of the version 3.x flex hybrid had to be modified to match changes in the IBM IC pinouts, and submission for fabrication should occur late in September. Additional irradiations of optical ICs and components are planned for September at CERN.

1.1.1.5 Modules

Dummy 8" wafers were sent to the bump bonding vendors. Dummy modules indium bumped) are being mounted on sectors for additional thermal cycling tests. Some of these modules were partly damaged in transit from Italy and a change in packaging for shipment will be necessary in the future.

1.1.1.1 Mechanics

1.1.1.1.1 Design

Milestone	Baseline	Previous	Forecast	Status
Cables/services CDR	20-Jun-01	--	10-Dec-01	Delayed (See #1)
Support tube CDR	20-Jun-01	--	16-Oct-01	Delayed (See #2)
Global Support FDR	16-Oct-01	--	16-Oct-01	On Schedule
Release bid for Support tube	4-Dec-01	--	5-Oct-02	Delayed (See #3)
Support tube FDR	10-Dec-01	--	26-Feb-02	Delayed (See #4)
Release bids for support	18-Dec-01	--	5-Oct-02	Delayed (See #5)

Note #1 Gap decision requires some redesign.

Note #2-5 Design scope increased to support beam pipe, many interfaces to be resolved with other systems.

Sally Seidel (University Of New Mexico)

The PP2/cable project is awaiting delivery of selected connectors and alternate Lemo connectors to verify mating/demating on a prototype panel. Delivery is expected at the end of September.

Murdock Gilchriese (Lawrence Berkeley Lab.)

Disk Sectors: Design is complete.

Disk Rings: Design is complete

Support Frame: Design is complete apart from final FEA taking into account final estimates of weights and support conditions. Location of strain relief elements for services also need to be defined in disk region.

1.1.1.1.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
Complete global support development/prototypes	16-Oct-01	--	16-Oct-01	On Schedule
Complete B-layer shell prototype	10-Dec-01	--	10-Dec-01	See Note #1
Support tube development complete	10-Dec-01	--	26-Feb-02	Delayed (See #2)

Note #1 The design of the B-layer support has been changed to eliminate this item.

Note #2 Design scope increased to support beam pipe, many interfaces to be resolved with other systems.

Neal Hartman (Lawrence Berkeley Lab.)

INSTALLATION MOCKUP

Parts for the friction tester are in fabrication, but have not been returned from the shop yet. All parts should be completed and assembled by the end of September. Test pieces of carbon fiber laminate (approximately 1 foot square) have been quoted by a fiber vendor. They will supply 6 of these plates, which will be 1/2 mm thick, quasi-isotropic, and made from approximately 80 Msi Modulus fiber. Some plates will be surfaced with non-woven glass "mat" which should make the surface smooth and electrically insulative. Each plate should be able to make 4 disks for the friction tester. These plates will also be used to test heater designs for the PST.

Work on the pixel mounts design has begun, but specific interfaces to the mockup have not been defined. Once a conceptual design has been worked out, attachment to the mockup will be addressed.

The Pixel mockup frame has been discussed with a contract engineer. Assuming time permits, he should begin reviewing the solid models within the next two weeks, submitting first fabrication drawings by the end of September. It is planned to have all parts for the mockup frame in the shops by the end of October, and then assembled shortly thereafter.

The tooling mandrel for the pixel support tube (PST) has been put out for quotes. The baseline is an aluminum tube approximately 18" in diameter with a 1" wall thickness, 2.75 m long (forward length). Quotes from 3 vendors should be available by early September. Quotes are also being acquired for the fiber plates that will be used to make the PST flange faces. These are thick laminates, up to 8 mm thick, 22" square, and the vendor supplying the test plates for the friction setup cannot handle the size. Other vendors and possible fibers are being investigated.

COOLING SERVICES

Welding of tubes and fittings sent to a local vendor have not been successful. Initially, the vendor tried welding tubing from the old batch, in nominal size. One weld was visibly defective, in that there were obvious holes in the fillet. The other weld appeared to be good, but on leak checking, it leaked off scale (above 10^{-6}) with helium. The vendor complained that clearance between the tube and fitting was too large (~250 microns radial). In response, tube samples from the new batch (annealed before bending, however) were sent to the vendor swaged to more closely match the fitting ID (within 50 microns radial clearance). One weld attempted with this tubing also failed, with visible holes and charring in the weld. Since previous results with an east coast laser welder had been excellent, work with the local vendor was suspended. In order to ascertain whether the new material batch is causing failures in the welding, new tube samples have been sent to the east coast vendor. In addition, a visit is planned to the east coast vendor to discuss tooling and fabrication of actual sector tubes. This will occur in middle September. In the meantime, another local vendor has been contacted, and will begin test welding some new tubes and fittings within a week.

Neat resin samples were irradiated to 25 Mrad in C_3F_8, and no visible "oozing" was observed. Samples were weighed before and after irradiation, were dried before hand, and contained 1% silane by weight (adhesion promoter). No discernible weight change was observed from the irradiation procedure. However, when left in humid conditions, the irradiated samples seemed to gain more weight (presumably moisture) than non-irradiated controls in the same environmental conditions. Though weight gain was

small, several neat resin samples are currently being irradiated without C_3F_8 to see if irradiation in the fluorocarbon changes the material's hygroscopic behavior. Initial results, however, suggest that irradiation is not a problem for the adhesive and adhesion promoter currently being used.

Three of 7 Aluminum/PEEK Luer lock fittings have been tested up to the thermal cycling stage in the testing regimen. Only 1 failure of 7 has been observed, and that was due to accidental mechanical destruction during re-tightening. Most likely the glue joint in this fitting was suspect. Three of the 6 remaining fittings have been irradiated but not tested. All four of the aluminum/aluminum Luer fittings have been tested up to the thermal cycling stage. The environmental chamber has been programmed for the prescribed thermal cycling, and has been tested suitably. Pressure cycling apparatus are currently being designed and fabricated. In addition, the new leak check temperature of -35C was successfully attained during testing with the use of liquid nitrogen in the leak checking apparatus. Since Luer Lock results have been so promising, only Luer and Variseal fittings are currently undergoing testing (Indium joint designs have been halted for the time being). Work now centers on reducing the size of the luer fitting and adapting it to laser welding, which should be done within the next month.

1.1.1.1.3 Production — Murdock Gilchriese (Lawrence Berkeley Lab.)

Disk Sectors

Tooling fabrication is proceeding. Evaluation/tests of the aluminum coolant tubes have been successful. The only significant concern at the moment is the quality of the carbon-carbon-faceplates. All faceplates were delivered and about 40% have been inspected. The quality of the resin impregnation is not high and is variable. This has been discussed with the vendor and we will attempt to add resin to 8 plates and the complete process will be evaluated during a site visit in early August.

Disk Rings

The final fabrication drawings for the disk rings, including tooling, were received and were under review at the end of the month.

1.1.1.2 Sensors

1.1.1.2.1 Design

Milestone	Baseline	Previous	Forecast	Status
Compl. Spec for production order release	12-Mar-01	--	15-Sep-01	See Note #1
ATLAS PM approval of production procurement	23-Jul-01	--	1-Oct-01	See Note #2
Release initial MC for sensors/testing	23-Jul-01	--	1-Oct-01	See Note #3

Note #1-3 Production is planned to begin in January 2002. Since there is considerable slack in the sensor schedule, this has no impact on the global schedule.

Note #2 Production is planned to begin in January 2002. Since there is considerable slack in the sensor

1.1.1.2.2 Development/Prototypes — Sally Seidel (University Of New Mexico)

Acceptance testing of pre-production wafers continued. CV measurements on tiles, single chips, and mini-chips are complete for all TESLA and CiS wafers. I-V_gate on GCD devices continued as well as the lengthy I-t studies (which require 12 hours per device). Thus far only one non-conforming wafer has been observed (this a TESLA device measured at Prague). A minor problem with mask alignment is being corrected. Use of the sensor production database has begun at all of the probing institutes.

TESLA reports an improved yield. The contract with CiS is being revised such that a greater fraction of 2-good-tile wafers will be purchased.

1.1.1.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
First Outer production wafers delivered	18-Jan-02	--	18-Jan-02	On Schedule

1.1.1.3 Electronics

1.1.1.3.1 Design

Milestone	Baseline	Previous	Forecast	Status
FE-I1 spec complete	16-May-01	--	1-Sep-01	Delayed (See #1)
Management contingency decision DMILL	9-Jan-02	--	9-Jan-02	On Schedule

Note #1 Specification has been started, and was supposed to be ready for June review. Testing of Analog Test chip and completion of FE-I has taken priority. Document will be completed after submission

K K Gan (Ohio State)

We continue to study the IBM optical dice, DORIC-I1. Ten dice have been characterized. All have good duty cycle. The delay between clock pulses depends on the input data but is within the specification. We can achieve PIN threshold for no bit error in the decoding as low as the DMILL die, ~ 30 uA average current, when the die is mounted on an opto-board. We observe that the pre-amp oscillates when there is no input signal. This could be due in part to the cross talk between the pads for input and output, PIN cathode and pre-amp+, which are located next to each other. The oscillation frequency depends on whether the digital part of the circuit is on or off. This could be due to the cross talk because of the close proximity of the input (PIN bypass capacitor and trace) and output (digital circuit). The layout of DORIC-I2 will be rearranged to reduce the cross talk.

We have built a new setup for the September irradiation studies (24 GeV protons at CERN). This setup uses a cold box and allows the irradiation of both VDC and DORIC simultaneously, thus doubling the statistics. The setup is purely electrical, i.e. no VCSEL or PIN. For the VDC, the setup is the same as in the previous irradiation but for the DORIC, it has been greatly improved. In the previous setup, the signal for the PIN inputs, after 20 m of cable, was reshaped with a commercial chip placed 1 m from the beam. This did not allow for an increase of the input signal, i.e. "PIN" current, as the DORIC degraded and in addition the commercial chip was also damaged in the irradiation. In the new setup, we do not reshape the

signal but greatly attenuate it with a voltage divider placed in close proximity of the die to emulate the tiny "PIN" signal. This allows us to increase the PIN current to compensate for the irradiation damage.

Kevin Einsweiler (Lawrence Berkeley Lab.)

We continue to place all of our design resources on the deep-submicron design effort. We are working on a better understanding of our IBM test chips, which continue to show several significant differences between simulations and measurements. The major difference is in the risetime of the preamplifier, where the testchip shows a small-signal risetime that is more than a factor of two worse than expected. These differences were not seen in our TSMC chips, based on essentially the same GDS file. This makes it much more difficult to explain the results in terms of extra parasitic capacitance on key nodes in the design. We intend to irradiate at least one IBM test chip later in Sept at the LBL Cyclotron (we missed our June irradiation date due to the CERN shipping delays for our chips). We have further extended our simulation efforts for these chips to simulate precisely what we measure, and still find large differences in the preamp risetime, which in turn lead to poor timewalk performance for the IBM chips. Two additional tasks remain to complete this work. The first task is to simulate a large part of the test chip with all extracted parasitics on all nodes (although the agreement between simulation and measurements for TSMC suggests that, although the parasitics for IBM are in general somewhat larger that for TSMC, this cannot be a major factor). We are also characterizing individual transistors from a test structure included in our run, and we will carefully compare these results with our IBM SPICE models to confirm that they accurately reproduce the devices in our MPW run. Finally, we have studied the IBM and TSMC fill algorithms. These algorithms are used by the foundry to make sure that all of the critical layers in the design (active, poly, and all metal layers) satisfy the required fill fractions for the reticle. Typically, additional metal structures are added by the foundry to make sure that the metal is uniformly distributed over the reticle. This uniformity is important for the polishing/planarization steps used in the processing. We were initially concerned that the addition of fill patterns in IBM could have created additional parasitic capacitances that would change the performance of the design. This does not seem to be the case, but further investigation is continuing.

Meanwhile, work is continuing on all aspects of the complete FE-I chip. The analog parts of the chip have now been completed and first LVS and DRC checks done. The only remaining required work is the final resizing of the capacitors in the bump-bond pad in order to provide the desired values. This is made more difficult by the less-than-perfect agreement between the extracted values from Cadence/Diva and the results of careful hand-calculations (plus the fact that IBM does not explicitly give the area and fringe components of the capacitances between layers). Nevertheless, we have agreed on a procedure to use for this, and only modest layout work remains to modify the current capacitor values. The remaining work is to integrate the optional blocks at the bottom of the chip (capacitance measurement circuit, overvoltage protection, and prototype regulators). An analog test chip, similar to the one submitted in our Feb and Mar prototype runs, will also be created from the final analog blocks in the FE chip. This will allow us to perform a more complete characterization of the FE performance in the lab, particularly as a function of capacitive load and leakage current. Study is now proceeding on a possible second version of the default front-end which would address some of our concerns (particularly threshold dispersion). Since this run contains two pixel FE chips in each reticle, we would like to benefit from this to learn as much as possible about the front-end design. The second front-end will most likely modify the feedback capacitance to provide a preamplifier gain that is twice as large as the default value. This appears to have minimal effect on timewalk performance, but should reduce the threshold dispersion by a factor of two, since this is dominated by VT matching issues in the preamp and second stage amplifier. We are confining the possible modifications to relatively simple and low-risk changes, as more significant changes would require many

additional weeks of time to validate and lay out. Such additional delays are not acceptable at this stage, as our highest priority must be to provide the collaboration with usable rad-hard chips early next year.

The digital part of the chip is complete, and undergoing final Verilog and Timemill simulations. This work should be complete within about two weeks. We anticipate putting together the reticle in the final week of Sept. The other chips in the reticle are somewhat further behind schedule. We expect to receive the final design files for the MCC on about Oct. 5, and we hope to receive the final design files for the VDC and DORIC by Sept 28. We are working on doing final DRC checks with the official Hercules DRC files used at CERN. This tool has already been validated on several previous submissions. We hope that this additional investment will minimize delays in beginning the fabrication of our wafers. IBM requires that all DRC errors in the final GDS file have a justification, and IBM must grant a waiver on a case-by-case basis. We would anticipate sending the final GDS file to IBM about Oct. 8, which should give us wafers back in mid-December.

As the pinout of the FE-I has become frozen, we are beginning to work on the necessary probe cards and support cards required for testing wafers, single die, and modules. All of these cards need to be updated, because of major changes to the pinout required to meet the production module mechanical envelopes. These cards will all be modified and re-fabricated over the next few months, in order to have everything ready in time for the returning wafers. We have designed our standard LVDS buffer chip to fit a standard SOIC28 package. This part will be used to provide rad-hard LVDS buffering and LVDS to CMOS conversion at our nominal operating voltage of 2.0V on all of our standard support cards.

In order to exercise the next generation of chips from ATMEL and IBM to the fullest extent possible, and in particular to develop the capability to label chips as "known good die", and be sure that this classification will remain true after exposure to the full radiation doses of ATLAS, we are developing an improved test system.

We have continued testing of the first PLL boards received. This work has struggled with limited manpower, but is finally receiving attention (and making progress). Although the pre-production ROD cards are not yet out for fabrication, John Joseph has been working to complete the PLL VHDL, and test and debug it in the lab. This work appears to be going well, and we anticipate being able to move on to testing of the PLL with real pixel chips within 1-2 weeks. All of the major blocks on the card are working properly, including on-board input and output FIFOs and the large histogramming SRAM. After this initial debugging is complete, additional VHDL will be added for testing the new FE-I and MCC-I chips, and the PC host software will be updated accordingly. We do not presently anticipate any major problems in completing this work in time for the testing of FE-I. However, we have uncovered several errors or omissions from the first PLL board that must be fixed before it is mass-produced. These include missing support for 80 Mbit links, a mirror-image connector geometry, and limitations from a 16-bit connection from VME to the FPGA. The most critical of these revisions will be made on our existing 3 prototype PLL boards, and then the schematics will be revised and an updated board layout will be done. The revised boards will not be available until late this year. This will limit the ability of outside groups (besides LBL and Bonn, who will receive the initial 3 prototype PLLs for wafer and chip testing) to perform testing of FE-I assemblies and is very unfortunate. We anticipate that this will cause much frustration on the part of our collaborators, but should not create any important additional delay in the project schedule.

We have now completed the PICT schematics and they have been crosschecked after all final modifications. The VHDL programming for the board has started, and a first pass at a new PLL-PICT slow-control protocol is being developed, along with all of the special commands to control the many chips

on the PICT from the PLL. The package geometries for all parts have been entered into Mentor. All parts have been ordered, including all revisions to the parts list as a result of schematic updates over the last month. We do not anticipate any parts delivery problems at this time. The layout of the board has been delayed by the ongoing work for the ROD pre-production prototype card. This has introduced what appears to be 2-3 weeks of delay in getting the PICT card out for fabrication. We hope that the layout of the PICT will begin again seriously within about one week. This will delay the board fabrication until mid-October, making it very difficult to deliver assembled cards by the end-October date that was our goal. However, with the present FE-I schedule, we are still cautiously optimistic that there will be PICTs with all VHDL and host software support in place in LBL and Bonn in time for initial FE-I wafer testing. However, it will be possible to perform first testing of FE-I with the new PLL and an old PCC card replacing the PICT. This will allow us only to check the core functions of the chip under 40 MHz operation, and not to perform all of the additional characterization provided by the PICT. We will also make sure that this backup solution is in place in case the PICT schedule slips further.

1.1.1.3.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
FE-D3 submitted	2-May-01	--	2-Dec-01	Delayed (See #1)
1st IBM prototype submitted (FE-I1)	26-Jul-01	17-Sep-01	8-Oct-01	Delayed (See #2)
FE-D3 wafers arrive	22-Aug-01	22-Aug-01	22-Dec-01	Delayed (See #3)
1st IBM prototype delivered	24-Oct-01	12-Nov-01	7-Dec-01	Delayed (See #4)
Complete initial wafer probe FE-I1	7-Nov-01	26-Nov-01	21-Dec-01	Delayed (See #5)
FE-D3 wafer tests complete	9-Jan-02	--	9-Jan-02	Delayed (See #6)
First bump bonded FE-I1 assemblies arrive	9-Jan-02	9-Jan-02	15-Feb-02	Delayed (See #7)

Note #1, 3, 6 We have delayed all further work on FE-D3 pending submission of FE-I1 and study of its performance. At the present time, no further DMILL submissions are foreseen unless significant problems are observed with 0.25u designs

Note #2, 5 Testing of the Analog Test chip has revealed large threshold dispersion. This must be improved before full submission. Other accumulated delays suggest a total ten-week delay in the submission date.

Note #4 See Note #2 above. Note that due to reduced foundry demand, the turnaround for IBM has been observed to be as low as 5 weeks, so the 8-week processing time assumed here should be reasonable.

Note #7 See Note#2 above. We are assuming a 6-week turnaround for the bump-bonding vendor. Significant processing of dummy wafers will be performed first to validate the processing of 8" wafers.

1.1.1.4 Flex Hybrids/Optical Hybrids

1.1.1.4.1 Design

Milestone	Baseline	Previous	Forecast	Status
Optical FDR	31-Jan-02	31-Jan-02	15-Feb-02	Delayed (See #1)

Note #1 Synchronized with pixel week in February.

Rusty Boyd (University of Oklahoma)

Flex Hybrid Design (UOK)

The design and layout of the flex hybrid v3 was completed in late July. The design files have been made available to the Pixel collaboration for review and comment. Flex hybrid v4 is thus about 90% complete. Work will continue on v4 after v3 has been submitted for fabrication. No problems are anticipated with prompt delivery of v3 and v4 flex, due to the current economic slump across the electronic sector. Compunetics assures us that they can begin fabrication as soon as they receive the files. Other vendors have been in contact with us asking for the current expected release date of the v4 design. We believe that we can have the final v3 files ready within two weeks of receiving word that the FE-I pin out is frozen. The v4 files should be ready within one month following.

1.1.1.4.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
Initial Flex 3.x tests complete	13-Dec-01	--	13-Dec-01	On Schedule

K K Gan (Ohio State)

We have fabricated a new opto-board for the September irradiation with 24 GeV protons at CERN. Due to the very late delivery of the Taiwan opto-packs, we can only get five out of the six optical links working. With all five links running simultaneously using 20 m fibers/power cables, the PIN current thresholds for no bit error are ~ 30-80 uA. This is quite satisfactory given that the opto-board is not optimized for the die layout and the VDC injects noise into the DORIC since they both are on the same dice. Mechanically, the system is also much sturdier because the 1 m radiation-hard fibers are protected with a furcation tube and the 20 m radiation-soft fibers/power cables are merged into a single hybrid cable using a shrink tube. This should make for much safer handling and reduced setup time.

Rusty Boyd (University of Oklahoma)

Flex Hybrid Development (UOK)

The high voltage capacitors irradiated at CERN PS during May of this year required some repair. We expect to be able to complete the tests in mid-September. These were irradiated under 700 VDC and will be tested both with and without voltage applied. The DAQ system used for testing the capacitors has been upgraded to speed analysis of the results.

We have completed assembly of v2 flex hybrids and the pigtails and an LBNL mini support card for these flex. We expect to begin test development for assembled flex circuits in early September. We are also assembling a connector interface card to allow rapid adaptation of the test system to v3 and v4 flex hybrids. We have enlisted the services of a physics graduate student for development of the Labview-based test system.

We are still awaiting simulation information on the expected power input requirements for FE-I. The final changes in the FE-I pin out will also have to be incorporated into the simulation model. Fortunately, we have built the simulation in blocks so that rebuilding the flex hybrid power bussing model should not be too

difficult. We have begun modeling the micro twisted pair cable that is anticipated to be used along the barrel staves for routing power and signals to/from PP0. We hope to obtain at least a qualitative idea of how the twist rate, distance and frequency affect the radiated signal in nearby circuits.

1.1.1.4.3 Production

Milestone	Baseline	Previous	Forecast	Status
Start initial production buy of components	13-Dec-01	--	13-Dec-01	On Schedule

1.1.1.5 Modules

1.1.1.5.2 Development/Prototypes — Maurice Garcia-Sciveres (Lawrence Berkeley Lab.)

LBL Module Assembly Status Report for September 4, 2001

Dummy Modules

Three more Alenia dummy bare modules have been obtained and assembled with flexes. Two of these were damaged in shipping from Genova.

They were sent in a gel pack (2 in on pack) and came loose in transit. Each module lost two FE chips. The remaining chips were probed at LBL and most have good connectivity. The 3 modules are being loaded on a prototype sector in preparation for thermal cycling.

Hot Modules

Two working hot modules, both IZM bumps, have been loaded on the same sector and preparations are in progress for a minimal system test.

Dummy Wafers

A total of 13 dummy FE 8" wafers have been delivered by Process Specialties. These wafers have PETEOS oxide passivation (0.5um) over 0.6um of aluminum. The lithography looks excellent. Six wafers are already at IZM and 5 or 6 are being sent to Alenia.

Wafer Thinning

A bumped 6" wafer has been thinned at APTEK to 125um with the back side polished and stress-relieved. This wafer can be safely handled without any support. It is flexible like a metal foil. The only problem is that the solvent used by APTEK to remove the wax used for holding the wafer during grinding has attached the protective photoresist. Because of this the photoresist was removed. Possibly wafers will have to be thinned without photoresist (this is what the vendor recommends). If this is done, the wafers may have to be coated to protect during dicing.

PP0

A service panel prototype is being constructed using G-10 instead of carbon fiber using existing version 1 PP0 prototypes.

PP1

A miniature connector type from Cristek Inc. is being explored as a possibility for PP1. The main issue is termination of aluminum wires and Cristek has agreed to do some process development.

Equipment

An Orthodyne Model 20 thick wire bonder has been received and is being commissioned. This will be used for the PP0-PP1 service panel and for the disk type 0 cables.

1.1.2 Silicon Strip System — Abe Seiden (University Of Calif. At Santa Cruz)

The first 35 production wafers from ATMEL were delivered to CERN and then distributed to the test sites (16 to UCSC, 15 to RAL, with 4 remaining at CERN so that they could perform an independent radiation qualification test on one chip per wafer using x-rays). There are as yet no data on yield from this production batch. ATMEL has established a delivery schedule which foresees approximately 100 wafers delivered every two weeks. This would result in delivery of the 520 wafers ordered by the end of this calendar year. It represents a delivery rate about twice as fast as in our baseline schedule. This would allow us to stay on schedule even if the yield is approximately half of the frame contract minimum value. Wafers made with the new epi vendor are expected to start arriving in November, at which time we can start making more informed yield projections.

Work on module production is continuing. A schedule for all the jigs has been made and work is progressing on these items. More work to finalize the burn-in procedure for hybrids is needed. This should be one of the items discussed at the October SCT week, with a goal of defining a burn-in specification which will be followed by all test sites. A final specification for the mechanical scheme to position and mount baseboards is still not in hand, with several options still being evaluated. A resolution of this issue is the most urgent item at present.

1.1.2.1 IC Electronics

1.1.2.1.1 Design — Alexander A. Grillo (University Of Calif. At Santa Cruz)

LBNL & UCSC

Work continued to reduce the ABCD wafer test time and to add tests of the chip I/O parametrics. The difficulty now is that production wafers are in hand and tester qualification has been completed. Therefore, care must be taken to qualify any test change and to implement the changes in such a way as to not disrupt the production test operation. A plan was agreed for a phased implementation with one minor change to be implemented immediately before production testing starts, more substantial changes to be implemented in late September after the first 35 production wafers have been tested but before large volumes of wafers arrive in mid-October. Final changes which will no longer collected full test data on failing chips will not be implemented until the end of the year after high statistics on production material has been obtained. Vitaliy Fadeyev from LBNL is responsible for implementing these changes.

Some work was also performed to try to understand some of the remaining questions from the test qualification data. In particular, the unexplained low rate of digital errors in otherwise good chips was investigated. The errors disappear on the SCIPP tester when the prober controller is turned off during testing. This indicates that the source of the problem is noise. Increasing the filtering on the chip power

lines also improved the problem but did not eliminate it. Work on this is continuing but for the time being we will continue to accept a low error rate (< -5%) for passing chips.

As was reported in June, Ned Spencer was asked by the SCT collaboration to help with a redesign of the hybrid for the forward module. As part of that work, Ned participated in a design workshop at Freiburg in August. The layout of the new (named K5) forward hybrid is nearly complete. All the electrical details have been completed with a few mechanical details remaining before the hybrid is submitted for fabrication.

1.1.2.1.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
Test Systems Complete	3-Aug-01	--	3-Oct-01	Delayed (See #1)

Note #1 The wafer test systems are operational and qualified for production. Some work is continuing to reduce test time and add some improved tests. It is expected that this will be complete by October when the large volume of production wafers starts to arrive.

Alexander A. Grillo (University Of Calif. At Santa Cruz)

LBNL & UCSC

The last 3 pre-production wafers were tested. Very little was accomplished with regard to the remaining radiation issues with the ABCD. This work is being done at CERN and by ATMEL and most Europeans were on vacation for the month. This work will have to continue in September.

1.1.2.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
Complete preproduction fab	28-Feb-01	--	10-Aug-01	Completed (See #1)
First Lots Delivered	23-Nov-01	23-Nov-01	27-Aug-01	Completed
1st ICs Avail for Prod Hybrids	4-Jan-02	--	4-Jan-02	On Schedule

Note #1 The last of the 5 pre-production lots was delivered with one out of spec fab parameter. We gave Atmel a conditional waiver in that we said we would first test the wafers and then determine to accept them only if the out of spec parameter did not effect yield or performance. Atmel has also delivered some extra wafers to augment the last lots which did yield poorly. All wafers have been tested. The extra wafers delivered by ATMEL were sufficient to complete the 40wafer pre-production order.

Alexander A. Grillo (University Of Calif. At Santa Cruz)

LBNL & UCSC

The first batch of 35 ABCD production wafers was delivered by ATMEL in August. They were delivered approximately 2 weeks late. ATMEL stated that the cause was a delay in obtaining their x-ray data on the wafers to certify the lots. The one good point was that they followed the accepted plan to not ship until the lot could be certified with the x-ray data. Sixteen of these wafers were received at UCSC on 31-Aug. Fifteen wafers were in transit to RAL and four wafers were held at CERN for ATLAS-SCT to perform our own x-ray tests on 4 ABCD chips. This is in accordance with the revised QA plan as recommended by the ABCD PRR committee.

Three students have been trained to handle wafers and perform wafer testing. One more student will be hired and trained to complete the necessary crew. They will work staggered short shifts during the academic year to keep the testing on schedule.

1.1.2.2 Hybrids/Cables/Fanouts

1.1.2.2.1 Design

Milestone	Baseline	Previous	Forecast	Status
ATLAS PM Approval of Maj Procs	20-Aug-01	--	20-Aug-01	Completed
Hybrid/Module Production Readiness Review	3-Sep-01	--	3-Sep-01	On Schedule
Complete Award Hybrid Contracts	14-Sep-01	--	14-Sep-01	On Schedule

1.1.2.2.2 Development & Prototype Fabrication — Carl Haber (Lawrence Berkeley Lab.)

The wirebonding process was performed on a K4 version hybrid. Results were good with ~8 gram or higher pulls. New machine settings were determined. The fanout bonding process was documented and the bonding technician was briefed on how to proceed.

A new concern emerged. Quality seems to vary on the line work on the fanouts. A letter was sent to Japan enquiring about this but no reply was received.

Work continued on the folding fixture.

The K4 hybrid was tested. It functions digitally but one of 12 chips shows higher noise. The origin of this is not understood. A probing arrangement was set up and various offset voltages were measured chip by chip. In this reqard the offending chip seems normal.

Thermal profiles were studied on the hyrbid in an attempt to measure temperature differences between the thermistor and the chips.

1.1.2.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
1st Preproduction Hybrids Avail for Mod Assy	4-Jun-01	--	15-Sep-01	Delayed (See #1)
Compl Preproduction Assy	13-Aug-01	--	21-Oct-01	Delayed (See #2)
Compl Testing of Preprod Hybrid	3-Sep-01	--	21-Oct-01	Delayed (See #3)

Note #1 This will follow the hybrid design review and is set by Japanese procurement schedule. The FDR is complete but some minor mods have been circulated.

Note #2-3 Set by date of item1 above.

Carl Haber (Lawrence Berkeley Lab.)

The concept for a flexible multi-purpose plate (MPP) to carry the hybrid through various stages of fabrication, test, and debug, was discussed. A design will be executed in the next month or so.

1.1.2.3 Module Assembly and Test

1.1.2.3.1 Design of Assembly & Test Tooling

Milestone	Baseline	Previous	Forecast	Status
Compl Design of Preprod Mod Assy/Test	3-Sep-01	3-Sep-01	3-Oct-01	Delayed (See #1)
Module PRR	3-Sep-01	3-Sep-01	1-Feb-02	Delayed (See #2)

Note #1 The pre-prod series awaits a resolution of the module fixation point problem. The design of the fixation point is a UK responsibility and we are dependant on that.

Note #2 Given the delay discussed in #1 above this is the current expected date for the US module assembly PRR.

Carl Haber (Lawrence Berkeley Lab.)

Additional drawings were received from RAL. The final design of the window frame is delayed until the issue of the baseboard fixation point can be resolved.

A request was sent to Japan for the design of the module holding tool.

A new design for the baseboard support plate was proposed by RAL and will probably be adopted.

1.1.2.3.2 Development & Prototypes

Carl Haber (Lawrence Berkeley Lab.)

The firmware for the new Z actuator was received and installed. The auto-focus code is now working well enough for use. The machine is in the process of recalibration and alignment. The dark box has been received and is being wired and installed. Documentation is complete on the wafer probing software. Work continues on the dummy wafers. Shipment from vendor is now expected mid-September. A set of wafers with a defect in the fiducial was found and seen to "fool" the pattern recognition code. This has been discussed with Manchester and a sample will be dispatched to them.

1.1.2.3.3 Production

Milestone	Baseline	Previous	Forecast	Status
Complete Preproduction Module Assembly	30-Jul-01	30-Oct-01	30-Nov-01	Delayed (See #1)
Complete Preproduction Module Testing	3-Sep-01	30-Oct-01	15-Nov-01	Delayed (See #2)
Start Full Strip Module Production	7-Jan-02	7-Jan-02	1-Feb-02	Delayed (See #3)

Note #1-2 Require pre-production hybrids which won't be available until the end of summer. Requires resolution of module fixation point design.

Note #3 Defined as date of module assembly PRR.

Carl Haber (Lawrence Berkeley Lab.)

Ordering of multiple sets of assembly fixtures awaits resolution of the module fixation problem. The production glue pattern was programmed into the machine. Additional Alumina baseboards for the pre-PRR series were received.

1.1.3 ROD Design & Fabrication — Dick Jared (Lawrence Berkeley Lab.)

The VHDL code for the ROD has been updated for the formatter FPGA. This change was needed to improve the utilization of the FPGA. The changes have resulted in a change of utilization from 92% to 74%. These changes are currently under test VHDL to test the wiring on the ROD has been written and is still under test. This is special code that allows the test stand to test the integrity of the copper traces on the ROD. The code will be used in production.

The ROD is being upgraded to the production model. The Schematics have been upgraded to the production model. Layout of the PC has progressed to auto routing. Production model cards are scheduled to be fabricated in early October. These cards will be needed for user evaluation of the ROD.

Code for the master DSP primitive that configures the front modules has been written and will be tested.

1.1.3.4 ROD Test Stand

1.1.3.4.3 SCT/Pixel Test Stand Software

Milestone	Baseline	Previous	Forecast	Status
Production Diagnostic Test Stand Completed	29-Sep-00	29-Aug-01	29-Oct-01	Delayed (See #1)

Note #1 The test stand software is completely functional for the production testing. This software will be updated for more efficiency in the next few months. The remaining testing is of the hardware (fabricated) to loop back the outputs to the FIFOs at the input to the ROD. The loop back cards are used to verify the output data quality. These loop back cards will be tested when more RODs are fabricated. Jan Valenta will arrive at LBL from Academy of Sciences of the Czech Republic in late September to complete the

work of Lukas Tomasek. Lukas will continue to support the effort from the Czech Republic till October and train Jan. No schedule impacts are forecasted.

1.1.3.6 ROD Prototype Evaluation

1.1.3.6.3 User Evaluation of ROD in Europe

Milestone	Baseline	Previous	Forecast	Status
SCT ATLAS Final Design Review	11-Jun-01	--	15-Nov-01	Delayed (See #1)
SCT ROD User Evaluation Complete	1-Oct-01	--	15-Apr-02	Delayed (See #2)
Pixel ATLAS Final Design Review	1-Jan-02	--	1-Jan-02	On Schedule

Note #1 The production model card are due to be fabricated and tested at LBL (3 ea.) by Oct. 30 2001. They will then be sent to Cambridge for testing to be completed by early November. The date for the review is predicated on the completion of the Cambridge test.

Note #2 The complete user evaluation is predicated as completion of the production model of the BOC and ROD. The prototype TIM will be used for the testing. The limiting factor is completion of the initial SCT DAQ. The SCT DAQ prototype is schedule to be completed in October of 2001 and the usable DAQ will be ready in January of 2002. The DAQ and cards will be used at CERN in December 2001 to early April 2002 to verify that the SCT Off Detector Electronics function as expected.

1.1.3.7 ROD Production Model

1.1.3.7.1 Updating of ROD to Production Model

Milestone	Baseline	Previous	Forecast	Status
SCT ATLAS ROD PRR	1-Oct-01	15-Apr-02	15-Nov-02	Delayed (See #1)

Note #1 The PRR is contingent on completion of the user evaluation. Please see 1.1.3.6.3 SCT ROD user evaluation complete for details.

1.1.3.7.3 Evaluation of Production Model

Milestone	Baseline	Previous	Forecast	Status
Release Production Dwg/Specs	16-May-01	15-Aug-01	10-Sep-01	Delayed (See #1)
Pixel ROD Design complete	14-Jun-01	--	15-Nov-01	Delayed (See #2)
Release Production Bids	4-Jul-01	20-Aug-01	20-Sep-01	Delayed (See #3)
Bid Evaluation Complete	15-Aug-01	7-Sep-01	15-Sep-01	Delayed (See #4)

Note #1 The current progress show that the drawing will not be ready till 10 September of 2001. This was caused by the extended time required to debug the proto ROD. Production is not expected to slip past the macro assembly site need date.

Note #2 The production model is scheduled to be tested at LBL and Cambridge by November 15 2001.

Note #3 The first bid to be released is for the Production model and 5% production of PC cards (25 ea.). The large production bid will not be released till the user evaluation at CERN system test is complete. These card are needed for the system test at CERN and evaluation of the ROD at the macro assembly sites.

Note #4 The delay will have no impact on needs.

1.1.3.8 ROD Fabrication

1.1.3.8.1 ROD 5% Production

Milestone	Baseline	Previous	Forecast	Status
Begin First End Cap SCT Module Ass/Test	25-Nov-01	--	25-Feb-02	Delayed (See #1)
Begin First Barrel SCT Module Ass/Test	27-Dec-01	--	27-Dec-01	Delayed (See #2)

Note #1-2 Projected by survey of the macro assembly sites.

1.1.3.8.2 SCT ROD Production

Milestone	Baseline	Previous	Forecast	Status
ROD 45% Production complete	16-Jan-02	16-Jan-02	16-Jul-02	Delayed (See #1)

Note #1 The production cannot start until ATLAS has significant user evaluation and a review of the SCT Off-detector Electronics.

1.2 TRT

Milestones with changed forecast dates:

1.2.1.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
HV Plates (Module #3) CUM #5 Available	28-Feb-01	28-Aug-01	28-Sep-01	Delayed (See #1)
HV Plates (Module #2) CUM #14 Available	30-Apr-01	30-Aug-01	30-Sep-01	Delayed (See #2)
HV Plates (Module #3) CUM #11 Available	30-Apr-01	30-Sep-01	28-Aug-01	Completed
HV Plates (Module #2) CUM #15 Available	31-May-01	1-Sep-01	1-Nov-01	Delayed (See #3)
Shells (Module #3) CUM #12 Available	31-May-01	31-Aug-01	31-Oct-01	Delayed (See #4)
Module Assy #3 Duke & IU Module Assy CUM #4 Complete	31-May-01	1-Sep-01	1-Nov-01	Delayed (See #5)
Module Assy #1 IU Module Assy CUM #9	31-May-01	1-Sep-01	28-Aug-01	Completed

Complete				
HV Plates (Module #1) CUM #16 Available	31-May-01	1-Sep-01	28-Aug-01	Completed
CUM #9 Test Complete	31-May-01	1-Sep-01	1-Dec-01	Delayed (See #6)
CUM #32 Kit Available	31-May-01	1-Sep-01	1-Dec-02	Delayed (See #7)
Module Assy #2 Duke Module Assy CUM #9 Complete	31-May-01	31-Aug-01	1-Nov-01	Delayed (See #8)
HV Plates (Module #1) CUM #17 Available	29-Jun-01	29-Aug-01	29-Sep-01	Delayed (See #9)
HV Plates (Module #2) CUM #17 Available	29-Jun-01	29-Aug-01	29-Nov-01	Delayed (See #10)
Shells (Module #1) CUM #17 Available	29-Jun-01	29-Aug-01	29-Nov-01	Delayed (See #11)
Shells (Module #2) CUM #17 Available	29-Jun-01	29-Aug-01	29-Nov-01	Delayed (See #12)
Shells (Module #3) CUM #13 Available	29-Jun-01	29-Sep-01	29-Nov-01	Delayed (See #13)
CUM #27,943 Available from CERN	31-Jul-01	31-Aug-01	1-Sep-01	Delayed (See #14)
CUM #20,665 Available from Hampton	31-Jul-01	31-Aug-01	1-Sep-01	Delayed (See #15)
Wire Joints -2 CUM #15 (200/m) Available	31-Jul-01	31-Aug-01	1-Nov-01	Delayed (See #16)
Module Assy #1 IU Module Assy CUM #15 Complete	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #17)
Wire Joints -1 CUM #40 (600/m) Available	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #18)
HV Plates (Module #1) CUM #20 Available	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #19)
CUM #48 Kit Available	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #20)
CUM #30,243 Available from CERN	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #21)
CUM #23,000 Available from Hampton	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #22)
HV Plates (Module #2) CUM #19 Available	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #23)
Wire Joints -2 CUM #17 (200/m) Available	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #24)
HV Plates (Module #3) CUM #15 Available	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #25)
Shells (Module #3) CUM #15 Available	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #26)
Shells (Module #2) CUM #19 Available	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #27)
Shells (Module #1) CUM #20 Available	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #28)
Module Assy #3 Duke & IU Module Assy CUM #10 Complete	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #29)
Module Assy #2 Duke Module Assy CUM #15 Complete	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #30)
Production Modules A Testing Complete	30-Sep-01	30-Sep-01	30-Oct-01	Delayed (See #31)
Shells (Module #3) CUM #10 Available	30-Sep-01	30-Sep-01	30-Aug-01	Completed

Note #1 Waiting on HV plates.
Note #2 American Circuits working on backlog of approved plates.
Note #3, 5-8 Delayed due to pause.
Note #4 Shells are keeping up with production but are delayed wrt schedule.

Note #9-30 Delayed.
Note #31 Mapping facility at Hampton should be completed in October.

1.2.5.1.2 Prototype

Milestone	Baseline	Previous	Forecast	Status
ASDBLR Design Frozen	13-Jul-01	15-Sep-01	15-Oct-01	Delayed (See #1)

Note #1 The new "properly processed" wafers arrived in mid July and plastic packaged parts were delivered on the 31st. Preliminary measurements indicate that matching and other functionality is as expected (hoped), however, the noise measurements are not as good as the SPice simulations would have indicated. There is something not yet understood about either the design or the process and we need to be sure that we understand where the excess noise is coming from and to what level we can tolerate somewhat more input noise before we can consider the design frozen. Until we have such an understanding we can not be certain that some design changes will be necessary. The 15 Oct. date is merely a guess - were we to have confidence in our understanding anytime before mid November it would be unlikely to have any effect on the overall schedule as the PRR must wait for information from large scale tests before it can proceed and those tests will occupy several months and are independent (to a very large degree) on the actual noise floor.

1.2.5.1.3 Production (Qty = 64,000 + 32,000 Chips)

Milestone	Baseline	Previous	Forecast	Status
Management Contingency Go-Ahead	2-Jul-01	15-Aug-01	15-Sep-01	Delayed (See #1)

Note #1 We would have hoped that this was on schedule - sort of not entirely under our control though. The schedule is still not under our control. Right now the increased noise leaves us uncertain about when we will actually be fully confident to go forward with pre-production and production purchases, but if the contingency go-ahead is delayed much more, then we will certainly not be able to meet the ATLAS milestones or we will have to pay much more. We were recently notified that it was necessary that the project office "be aware of the overall chip yield" prior to any consideration of release of contingency - note that this was sent to us 28 days AFTER the project office stipulated date of contingency go-ahead. The yield numbers available to us (and the project office) have not changed greatly over the last few months - still ~45% overall yield from the first wafer run - and now we have preliminary yields on the 00 run, better because of matching improvements (roughly 55% for the same level of cuts as the 45% for the 99 version but the confidence in any of these numbers is fairly small as the number of lots is only two. The noise question confuses this a bit, but is mostly a question of how we balance what we can live with what we are willing to change - in the worst case we revert to the single stripe transistors and pare down the input protection system. The actual order will, nevertheless, have to be based on fairly conservative yield numbers or we will risk being stuck going back for additional wafers at a MUCH higher per wafer cost. Given that the cost estimates in the January 01 BCP are based on such moderately conservative yield numbers, it is highly unlikely that there would be any change in the requested (or prudent) purchase. Given that we now have evidence for some improvement in parametric yield the only plausible question remaining before Go-Ahead is whether or not the measured noise is understood and can be tolerated - it is not clear that gating the Contingency release (as opposed to the actual purchase AFTER the PRR) is wise.

1.2.1 Barrel Mechanics

1.2.1.1 Barrel Module — Ken McFarlane (Hampton University)

No special difficulties were encountered, in component preparation. See detail below.

Harold Ogren (Indiana University)

Design work on the space frame and on details of the module envelopes continues. This is closely coupled to the small changes in the cooling plate design that will be required. Work was also done on the mapping facility at Hampton.

1.2.1.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
CUM #23,343 Available from CERN	28-Feb-01	--	28-Aug-01	Completed
HV Plates (Module #3) CUM #5 Available	28-Feb-01	28-Aug-01	28-Sep-01	Delayed (See #1)
HV Plates (Module #2) CUM #1 Available	30-Mar-01	--	30-Aug-01	Completed
CUM #27 Kit Available	30-Apr-01	--	30-Sep-01	Delayed (See #2)
CUM #5 Test Complete	30-Apr-01	--	30-Sep-01	Delayed (See #3)
HV Plates (Module #2) CUM #1 Available	30-Apr-01	30-Aug-01	30-Sep-01	Delayed (See #4)
HV Plates (Module #3) CUM #1 Available	30-Apr-01	30-Sep-01	28-Aug-01	Completed
CUM #32 Kit Available	31-May-01	1-Sep-01	1-Dec-02	Delayed (See #5)
CUM #9 Test Complete	31-May-01	1-Sep-01	1-Dec-01	Delayed (See #6)
HV Plates (Module #1) CUM #1 Available	31-May-01	1-Sep-01	28-Aug-01	Completed
HV Plates (Module #2) CUM #1 Available	31-May-01	1-Sep-01	1-Nov-01	Delayed (See #7)
HV Plates (Module #3) CUM #1 Available	31-May-01	--	31-Oct-01	Delayed (See #8)
Module Assy #1 IU Module Assy CUM # Complete	31-May-01	1-Sep-01	28-Aug-01	Completed
Module Assy #2 Duke Module Assy CUM #9 Complete	31-May-01	31-Aug-01	1-Nov-01	Delayed (See #9)
Module Assy #3 Duke & IU Module Ass CUM #4 Complete	31-May-01	1-Sep-01	1-Nov-01	Delayed (See #10)
Shells (Module #1) CUM #16 Available	31-May-01	--	31-Aug-01	Completed
Shells (Module #2) CUM #15 Available	31-May-01	--	31-Aug-01	Completed
Shells (Module #3) CUM #12 Available	31-May-01	31-Aug-01	31-Oct-01	Delayed (See #11)
CUM #37 Kit Available	29-Jun-01	--	29-Jun-02	Delayed (See #12)
HV Plates (Module #1) CUM #1 Available	29-Jun-01	29-Aug-01	29-Sep-01	Delayed (See #13)
HV Plates (Module #2) CUM #1	29-Jun-01	29-Aug-01	29-Nov-01	Delayed (See #14)

Available

HV Plates (Module #3) CUM #1 Available	29-Jun-01	--	29-Oct-01	Delayed (See #15)
Module Assy #1 IU Module Assy CUI #11 Complete	29-Jun-01	--	29-Sep-01	Delayed (See #16)
Module Assy #2 Duke Module Assy CUI #11 Complete	29-Jun-01	--	29-Sep-01	Delayed (See #17)
Module Assy #3 Duke & IU Module Ass CUM #6 Complete	29-Jun-01	--	29-Sep-01	Delayed (See #18)
Shells (Module #1) CUM #17 Available	29-Jun-01	29-Aug-01	29-Nov-01	Delayed (See #19)
Shells (Module #2) CUM #17 Available	29-Jun-01	29-Aug-01	29-Nov-01	Delayed (See #20)
Shells (Module #3) CUM #13 Available	29-Jun-01	29-Sep-01	29-Nov-01	Delayed (See #21)
CUM #25,643 Available from CERN	30-Jun-01	--	30-Aug-01	Completed
Mangement Contingency Go-Ahead	2-Jul-01	--	2-Oct-01	Delayed (See #22)
CUM #20,665 Available from Hampton	31-Jul-01	31-Aug-01	1-Sep-01	Delayed (See #23)
CUM #27,943 Available from CERN	31-Jul-01	31-Aug-01	1-Sep-01	Delayed (See #24)
CUM #42 Kit Available	31-Jul-01	--	31-Oct-01	Delayed (See #25)
HV Plates (Module #1) CUM #1 Available	31-Jul-01	--	1-Sep-01	Delayed (See #26)
HV Plates (Module #2) CUM #1 Available	31-Jul-01	--	1-Sep-01	Delayed (See #27)
HV Plates (Module #3) CUM #1 Available	31-Jul-01	--	31-Dec-01	Delayed (See #28)
Module Assy #1 IU Module Assy CUI #13 Complete	31-Jul-01	--	1-Sep-01	Delayed (See #29)
Module Assy #2 Duke Module Assy CUI #13 Complete	31-Jul-01	--	1-Sep-01	Delayed (See #30)
Module Assy #3 Duke & IU Module Ass CUM #8 Complete	31-Jul-01	--	1-Nov-01	Delayed (See #31)
Shells (Module #1) CUM #18 Available	31-Jul-01	--	1-Sep-01	Delayed (See #32)
Shells (Module #2) CUM #18 Available	31-Jul-01	--	1-Sep-01	Delayed (See #33)
Shells (Module #3) CUM #14 Available	31-Jul-01	--	1-Sep-01	Delayed (See #34)
Wire Joints -2 CUM #15 (200/m) Available	31-Jul-01	31-Aug-01	1-Nov-01	Delayed (See #35)
CUM #1 Kit Available	31-Aug-01	--	31-Aug-01	Completed
CUM #23,000 Available from Hampton	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #36)
CUM #30,243 Available from CERN	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #37)
CUM #48 Kit Available	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #38)
HV Plates (Module #1) CUM #2 Available	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #39)

HV Plates (Module #2) CUM #1 Available	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #40)
HV Plates (Module #3) CUM #1 Available	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #41)
Module Assy #1 IU Module Assy CUI #15 Complete	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #42)
Module Assy #2 Duke Module Assy CUI #15 Complete	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #43)
Module Assy #3 Duke & IU Module Ass CUM #10 Complete	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #44)
Shells (Module #1) CUM #20 Available	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #45)
Shells (Module #2) CUM #19 Available	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #46)
Shells (Module #3) CUM #15 Available	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #47)
Wire Joints -1 CUM #40 (600/m) Available	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #48)
Wire Joints -2 CUM #17 (200/m) Available	31-Aug-01	31-Aug-01	31-Oct-01	Delayed (See #49)
CUM #25,400 Available from Hampton	28-Sep-01	--	28-Sep-01	Delayed (See #50)
CUM #32,543 Available from CERN	28-Sep-01	--	28-Sep-01	Delayed (See #51)
CUM #54 Kit Available	28-Sep-01	--	28-Sep-01	Delayed (See #52)
HV Plates (Module #1) CUM #2 Available	28-Sep-01	--	28-Sep-01	Delayed (See #53)
HV Plates (Module #2) CUM #2 Available	28-Sep-01	--	28-Sep-01	Delayed (See #54)
HV Plates (Module #3) CUM #1 Available	28-Sep-01	--	28-Sep-01	Delayed (See #55)
Module Assy #1 IU Module Assy CUI #17 Complete	28-Sep-01	--	28-Sep-01	Delayed (See #56)
Module Assy #2 Duke Module Assy CUI #17 Complete	28-Sep-01	--	28-Sep-01	Delayed (See #57)
Module Assy #3 Duke & IU Module Ass CUM #12 Complete	28-Sep-01	--	28-Sep-01	Delayed (See #58)
Shells (Module #1) CUM #21 Available	28-Sep-01	--	28-Sep-01	Delayed (See #59)
Shells (Module #2) CUM #21 Available	28-Sep-01	--	28-Sep-01	Delayed (See #60)
Shells (Module #3) CUM #16 Available	28-Sep-01	--	28-Sep-01	Delayed (See #61)
Wire Joints -1 CUM #44 (600/m) Available	28-Sep-01	--	28-Sep-01	Delayed (See #62)
Wire Joints -2 CUM #19 (200/m) Available	28-Sep-01	--	28-Sep-01	Delayed (See #63)
CUM #25 Test Complete	30-Sep-01	--	31-May-02	Delayed (See #64)
Production Modules A Testing Complete	30-Sep-01	30-Sep-01	30-Oct-01	Delayed (See #65)
Shells (Module #3) CUM #10 Available	30-Sep-01	30-Sep-01	30-Aug-01	Completed

CUM #27,800 Available from Hampton	31-Oct-01	--	31-Oct-01	On Schedule
CUM #31 Test Complete	31-Oct-01	--	31-Oct-01	On Schedule
CUM #34,843 Available from CERN	31-Oct-01	--	31-Oct-01	On Schedule
CUM #60 Kit Available	31-Oct-01	--	31-Oct-01	On Schedule
HV Plates (Module #1) CUM #2 Available	31-Oct-01	--	31-Oct-01	On Schedule
HV Plates (Module #2) CUM #2 Available	31-Oct-01	--	31-Oct-01	On Schedule
HV Plates (Module #3) CUM #1 Available	31-Oct-01	--	31-Oct-01	On Schedule
Module Assy #1 IU Module Assy CUI #19 Complete	31-Oct-01	--	31-Oct-01	On Schedule
Module Assy #2 Duke Module Assy CUI #19 Complete	31-Oct-01	--	31-Oct-01	On Schedule
Module Assy #3 Duke & IU Module Ass CUM #14 Complete	31-Oct-01	--	31-Oct-01	On Schedule
Modules Production A Complete	31-Oct-01	--	31-Oct-01	On Schedule
Shells (Module #1) CUM #22 Available	31-Oct-01	--	31-Oct-01	On Schedule
Shells (Module #2) CUM #22 Available	31-Oct-01	--	31-Oct-01	On Schedule
Shells (Module #3) CUM #17 Available	31-Oct-01	--	31-Oct-01	On Schedule
Wire Joints -1 CUM #48 (600/m) Available	31-Oct-01	--	31-Oct-01	On Schedule
Wire Joints -2 CUM #21 (200/m) Available	31-Oct-01	--	31-Oct-01	On Schedule
Wire Joints -1 CUM #100 (600/m Available	29-Nov-01	--	29-Nov-01	On Schedule
CUM #1 Test Complete	30-Nov-01	--	30-Nov-01	On Schedule
CUM #30,100 Available from Hampton	30-Nov-01	--	30-Nov-01	On Schedule
CUM #37 Test Complete	30-Nov-01	--	30-Nov-01	On Schedule
CUM #37,143 Available from CERN	30-Nov-01	--	30-Nov-01	On Schedule
CUM #66 Kit Available	30-Nov-01	--	30-Nov-01	On Schedule
HV Plates (Module #1) CUM #2 Available	30-Nov-01	--	30-Nov-01	On Schedule
HV Plates (Module #2) CUM #2 Available	30-Nov-01	--	30-Nov-01	On Schedule
Module Assy #1 IU Module Assy CUI #21 Complete	30-Nov-01	--	30-Nov-01	On Schedule

Module Assy #2 Duke Module Assy CUM #21 Complete	30-Nov-01	--	30-Nov-01	On Schedule
Module Assy #3 Duke & IU Module Ass CUM #15 Complete	30-Nov-01	--	30-Nov-01	On Schedule
Shells (Module #1) CUM #24 Available	30-Nov-01	--	30-Nov-01	On Schedule
Shells (Module #2) CUM #23 Available	30-Nov-01	--	30-Nov-01	On Schedule
Shells (Module #3) CUM #18 Available	30-Nov-01	--	30-Nov-01	On Schedule
Wire Joints -1 CUM #52 (600/m) Available	30-Nov-01	--	30-Nov-01	On Schedule
Wire Joints -2 CUM #23 (200/m) Available	30-Nov-01	--	30-Nov-01	On Schedule
CUM #32,500 Available from Hampton	31-Dec-01	--	31-Dec-01	On Schedule
CUM #39,443 Available from CERN	31-Dec-01	--	31-Dec-01	On Schedule
CUM #43 Test Complete	31-Dec-01	--	31-Dec-01	On Schedule
CUM #71 Kit Available	31-Dec-01	--	31-Dec-01	On Schedule
HV Plates (Module #1) CUM #2 Available	31-Dec-01	--	31-Dec-01	On Schedule
HV Plates (Module #2) CUM #2 Available	31-Dec-01	--	31-Dec-01	On Schedule
HV Plates (Module #3) CUM #1 Available	31-Dec-01	--	31-Dec-01	On Schedule
Module Assy #2 Duke Module Assy CUM #22 Complete	31-Dec-01	--	31-Dec-01	On Schedule
Module Assy #3 Duke & IU Module Ass CUM #16 Complete	31-Dec-01	--	31-Dec-01	On Schedule
Shells (Module #1) CUM #25 Available	31-Dec-01	--	31-Dec-01	On Schedule
Shells (Module #2) CUM #25 Available	31-Dec-01	--	31-Dec-01	On Schedule
Shells (Module #3) CUM #19 Available	31-Dec-01	--	31-Dec-01	On Schedule
Wire Joints -1 CUM #56 (600/m) Available	31-Dec-01	--	31-Dec-01	On Schedule
Wire Joints -2 CUM #25 (200/m) Available	31-Dec-01	--	31-Dec-01	On Schedule
CUM #35,000 Available from Hampton	31-Jan-02	--	31-Jan-02	On Schedule
CUM #41,743 Available from CERN	31-Jan-02	--	31-Jan-02	On Schedule
CUM #49 Test Complete	31-Jan-02	--	31-Jan-02	On Schedule
CUM #75 Kit Available	31-Jan-02	--	31-Jan-02	On Schedule
HV Plates (Module #1) CUM #2 Available	31-Jan-02	--	31-Jan-02	On Schedule

HV Plates (Module #2) CUM #2 Available	31-Jan-02	--	31-Jan-02	On Schedule
HV Plates (Module #3) CUM #2 Available	31-Jan-02	--	31-Jan-02	On Schedule
Module Assy #1 IU Module Assy CUM #24 Complete	31-Jan-02	--	31-Jan-02	On Schedule
Module Assy #2 Duke Module Assy CUM #24 Complete	31-Jan-02	--	31-Jan-02	On Schedule
Module Assy #3 Duke & IU Module Ass CUM #17 Complete	31-Jan-02	--	31-Jan-02	On Schedule
Shells (Module #1) CUM #26 Available	31-Jan-02	--	31-Jan-02	On Schedule
Shells (Module #2) CUM #26 Available	31-Jan-02	--	31-Jan-02	On Schedule
Shells (Module #3) CUM #20 Available	31-Jan-02	--	31-Jan-02	On Schedule
Wire Joints -1 CUM #60 (600/m) Available	31-Jan-02	--	31-Jan-02	On Schedule
Wire Joints -2 CUM #27 (200/m) Available	31-Jan-02	--	31-Jan-02	On Schedule

Note #1 Waiting on HV plates

Note #2 Successful shipment from Dubna

Note #3 Testing at Hampton still not operational

Note #4 American Circuits working on backlog of approved plates.

Note #5-7, 9-10 Delayed due to pause.

Note #8 Delayed due to HV 3 plates.

Note #11 Shells are keeping up with production but are delayed wrt schedule.

Note #12 Kits will follow HV plates.

Note #13-14, 17, 19-21, 23-63 Delayed.

Note #15 HV plates delayed.

Note #16 delayed due to pause and parts.

Note #18 Delayed due to HV plates.

Note #22 Delayed until October when our production rates will be clearer.

Note #64 This appears to be out of sequence.

Note #65 Mapping facility at Hampton should be completed in October.

Ken McFarlane (Hampton University)

1.2.1.1.3 Production

Staff

We expect to hire an additional tech in October; that will give have a total of 6 technicians (including the QA tech, who now does assembly work on tension plates and capacitor barrels).

1.2.1.1.3.1 Detector Elements

1.2.1.1.3.1.1 Straws

A shipment of straws has arrived, from JINR (Dubna). A shipment was requested from PNPI.

1.2.1.1.3.1.1.2 End sockets (end plugs)

1.2.1.1.3.1.1.4.1 Twister

1.2.1.1.3.1.1.4.2 Twister

1.2.1.1.3.1.1.8.2 Wire bushing (eyelet)

1.2.1.1.3.1.1.8.3 Crimp pin (taper pin)

1.2.1.1.3.1.1.8.5, 6 Gas connections

All purchase orders or contracts for the above components have been placed, and deliveries are on schedule. Revised drawings for new gas connections were received.

1.2.1.1.3.4 Assembly

Straw subassemblies

Production continued with no special difficulties.

Radiator packs

Production continued with no special difficulties.

Dividers

Production continued with no special difficulties.

Wire supports

Production continued with no special difficulties.

Capacitor Barrels

Produced as needed for tension-plate processing.

Tension plates

These are now processed as needed to create HV plate/TP kits.

HV plate testing and assembly with tension plates

Production continued with no special difficulties.

Capacitor Assembly

No activity this month. The final decision on capacitor type has not been made.

1.2.1.1.3.1.1.8.5, 6 Gas connections

Active gas fittings are produced as needed for TP/HV kits.

Seog Oh (Duke University)

X-ray Scanner

The x-ray scanning is back in business. The amplifiers on the new PCB are low in noise and oscillation free. We have mapped 2.08 and 1.02 (one of IU modules). From the measurement, there are no obvious problems with either module, although a few channels at the corner in 2.08 exhibit fairly large gain fluctuation. For the moment, we are not scanning any more modules due to lack of manpower. We are trying to locate personnel to help with the scanning. We can scan a type II module and produce the all the necessary plots within a week.

Wire Joint Ageing Study

This task is moving quite well. We have finished the test chamber construction. All the electronics are connected and tested. We are at the final leg of debugging the software and expecting to take the first data in a week. We should have some preliminary result by the October ATLAS meeting.

HV Plates

It seems that we may have finally tackled the type III dimensional problem. Three sets (six plates) of type III HV plates were machined and measured. The measurements showed that they met the specification. Moreover another 15 sets (30 plates) of type I plates were produced and measured. All plates except one met the specification. We will be giving the final go-ahead for the rest of plates soon.

Module Construction Status

Module 2.10

The mechanical construction is almost finished. Should be in the string station in a week.

Module 2.11

The mechanical construction has started.

Module 3.02

It is being strung. About ~20% of straws are strung.

Wire-joint production

The wire-joint production is moving well. Both stations are producing high quality wire-joints.

The number of joints produced is meeting LOB requirement.

Harold Ogren (Indiana University)

Module production

We completed three type 1 modules this month. Wire stringing rates continue to grow and rework and wire breakage is reducing. We have been typically stringing about 70-80 wires a day for two technicians. The rates are acceptable for type 1 and type 3. We are also introducing a rework line that will allow us to bring back a module for restringing without interrupting the existing lines.

The 16 ch tension tester was brought into operation, and the module 1.03 was measured prior to shipping this to Hampton. This will be done in a separate space in our tension testing area. We are beginning to learn how to do this final tension testing and add it to the tension database.

Of particular interest to us is the success of the leak checking production phase. We now have the glue sealing operations well in hand, and have been able to complete the leak checking of the last six modules with only one test. During this month we also completed the final checking of six modules.

Presently we are working on modules 1.16, 1.15, 1.14, 1.13, 1.12 while all others are being electrically tested or are complete.

We have successfully implemented a realtime SQL transfer of tension data to the database from the two stringing stations. This cuts down the work to maintain the tension data files, and give us direct feedback from any computer on current stringing status as well as historical data.

Shells

We have been working with Vision to arrange for a production schedule of 8 acceptable shells per month. This would allow us to complete the shell production by next May 2002. Vision has agreed to this schedule. We have acceptable inventory on type 3 and type 2 shells, but only a few weeks ahead on type 1 shells. Vision had a number of problems with the type 1 shells that have not passed first spec checks on the minimum diagonal distance due to a small distortion of the profile. We are working with them on this, and it now appears to be a prepreg roll dependent problem. The success of the reforming become much more important, and they are investigating the recent string of failures in this area. We are also working out the final phase contract with them, which requires ordering more material.

Radiator

The initial phase of the production of mats is completed. However, due to a slightly higher count of mats in each module, and the lack of spare material in the initial contract we now are organizing a follow up contract to produce an additional 8000 mats. (The original production was for 33,000.) They have agreed to extend the original contract, and we are working with them to maintain the mechanical punches. We now have an inventory of mats that will cover us until next summer, so this is not a critical item. We also have sufficient raw material.

Shipping containers.

We have purchased over 100 reinforced tubes that will be used for holding the completed modules and will serve a individual containers when the modules are shipped to CERN in groups of 5-6. The first shipping tubes are being prepared for the initial module shipment to Hampton. Inside foam panels, endcaps, and clamp rings are on order.

1.2.1.1.4 Beam Test — Ken McFarlane (Hampton University)

Dr. O. Keith Baker participated in the TRT beam test work in August-September 2001.

Harold Ogren (Indiana University)

CERN beam test shifts began the last week of August. Fred Luerhing and Pauline Gagnon took part in the test shifts, which will continue until the second week of September. We also a awaiting information on the reactor test of 1.01. This module has been removed from the reactor and should be cool enough for more testing in the month of September. All indications are good that it survived the 20 year LHC neutron dose intact and in working order.

1.2.5 TRT Electronics

1.2.5.1 ASD/BLR

1.2.5.1.1 Design — Richard Van Berg (University Of Pennsylvania)

Design activities are centered around trying to understand the significant increase in noise measured in the ASDBLR00 (just returned) vs. the Spice prediction (~3300 e ENC vs. ~2200 e). While there is some suspicion of the new input protection structures, the Spice models would have to be seriously wrong to give the measured result. It is also possible that the Spice models for the transistor R_b are off or, more worrisome, that the R_b is not really controlled in the process. The observed noise levels are high enough to be very worrisome, but are probably within the range of useable values (possibly implying a small gain tweak to the chamber).

In addition to remodeling and careful examination of the circuit, we are having some of the input structures modified via ion beam in order to try to separate out possible candidate causes. We have also scheduled a meeting with factory representatives for early September to discuss this issue.

1.2.5.1.2 Prototype

Milestone	Baseline	Previous	Forecast	Status
ASDBLR Design Frozen	13-Jul-01	15-Sep-01	15-Oct-01	Delayed (See #1)
Select Final Electronic Design	31-Aug-01	--	31-Aug-01	Completed (See #2)
Production Readiness Review	11-Jan-02	--	11-Jan-02	On Schedule
Start Production	18-Jan-02	--	18-Jan-02	On Schedule

Note #1 The new "properly processed" wafers arrived in mid July and plastic packaged parts were delivered on the 31st. Preliminary measurements indicate that matching and other functionality is as expected (hoped), however, the noise measurements are not as good as the Spice simulations would have indicated. There is something not yet understood about either the design or the process and we need to be sure that we understand where the excess noise is coming from and to what level we can tolerate somewhat more input noise before we can consider the design frozen. Until we have such an understanding we cannot be certain that some design changes will be necessary. The 15 Oct. date is merely a guess - were we to have confidence in our understanding anytime before mid November it would be unlikely to have any effect on the overall schedule as the PRR must wait for information from large scale tests before it can proceed and those tests will occupy several months and are independent (to a very large degree) on the actual noise floor.

Note #2 Insofar as this milestone was meant to indicate a choice between a one chip and two chip solution, that is long since past and decided. However, were this to be updated to refer to a choice between DMILL and DSM DTMROC designs, then such a choice could not be made until we had samples of the DSM chip (working) or a lot of found money (Powerball?)- the first condition is likely (but not assured) in early 2002.

Richard Van Berg (University Of Pennsylvania)

Five wafers of the ASDBLR00 have been packaged in plastic TQFP and most of those have been tested at least once. Except for the question of noise figure (see above), the matching is significantly improved and the yields are noticeably better than for the ASDBLR99. Three more wafers are reserved for packaging in fine pitch ball grid arrays (FBGA). We have just recently gotten feedback from Signetics (Korea) that our preliminary designs are reasonable although they made some very small modifications. The FBGA packaging should be much better for both Barrel and End Cap use because of smaller parasitic inductances and capacitances and, for the Barrel at least, is really necessary to avoid the problems of using chip on board technology. Having gotten the initial feedback from Signetics we may be six or eight weeks away from being able to demonstrate whether or not FBGAs can fulfill their promise in this application.

There are about 1,000 ASDBLR00's packaged from these first five wafers. About 350 pieces have been run through the production test sequence and the functional yield is very similar to the ASDBLR99 yield of about 85%. The parametric yield (i.e. matching) is significantly improved for the measured chips - 59% with cuts at +/- 45 mV (about 0.5 fC) for channel thresholds vs. chip reduced mean threshold (i.e. mean of the 3fC channel thresholds for the seven closest channels on a chip). About 2% of these chips fail on

the high threshold matching on one channel. A more detailed report with plots of thresholds and distributions at various cut levels will be published in the near future.

In other areas, CERN is preparing new End Cap boards for the 00 chips to allow radiation and End Cap system testing to go forward. New radiation tests on the 99 versions of the chips showed little or no performance degradation with 10^{14} n/cm^2.

1.2.5.1.3 Production (Qty = 64,000 + 32,000 Chips)

Milestone	Baseline	Previous	Forecast	Status
Management Contingency Go-Ahead	2-Jul-01	15-Aug-01	15-Sep-01	Delayed (See #1)

Note #1 We would have hoped that this was on schedule - sort of not entirely under our control though. The schedule is still not under our control. Right now the increased noise leaves us uncertain about when we will actually be fully confident to go forward with pre-production and production purchases, but if the contingency go-ahead is delayed much more, then we will certainly not be able to meet the ATLAS milestones or we will have to pay much more. We were recently notified that it was necessary that the project office "be aware of the overall chip yield" prior to any consideration of release of contingency - note that this was sent to us 28 days AFTER the project office stipulated date of contingency go-ahead. The yield numbers available to us (and the project office) have not changed greatly over the last few months - still ~45% overall yield from the first wafer run - and now we have preliminary yields on the 00 run, better because of matching improvements (roughly 55% for the same level of cuts as the 45% for the 99 version but the confidence in any of these numbers is fairly small as the number of lots is only two. The noise question confuses this a bit, but is mostly a question of how we balance what we can live with with what we are willing to change - in the worst case we revert to the single stripe transistors and pare down the input protection system. The actual order will, nevertheless, have to be based on fairly conservative yield numbers or we will risk being stuck going back for additional wafers at a MUCH higher per wafer cost. Given that the cost estimates in the January 01 BCP are based on such moderately conservative yield numbers, it is highly unlikely that there would be any change in the requested (or prudent) purchase. Given that we now have evidence for some improvement in parametric yield the only plausible question remaining before Go-Ahead is whether or not the measured noise is understood and can be tolerated - it is not clear that gating the Contingency release (as opposed to the actual purchase AFTER the PRR) is wise.

Richard Van Berg (University Of Pennsylvania)

In order to keep the DMILL production times reasonable, it is necessary to order raw material (the SOI wafers) months in advance. We are preparing a PO to cover the initial pre-production material and expect to issue it in September so that production could, plausibly, begin immediately after a PRR in about January 2002.

1.2.5.2 DTM/ROC

1.2.5.2.1 Design

Richard Van Berg (University Of Pennsylvania)

No work on the DMILL DTMROC design at this time, but the DSM version is going ahead and seems to be converging with a probable submission date in October. All cells have been finished except for the DAC and some characterization of the memory that yet remains to be done. Prototype versions of the ternary receiver, the LVDS driver and receiver, the "Front End" and DLL, the test pulse, and subsections of the DAC have all been shown to work as designed. Final chip assembly is almost ready to proceed and it is possible that we will have a final netlist to check in mid September. Most of this work is going on at CERN, but Penn is responsible for the Ternary Receiver, LVDS driver, and Test Pulse cells - we also will help some with the DAC to maintain schedule.

1.2.5.2.2 Prototype **Richard Van Berg (University Of Pennsylvania)**

We have had five wafers of DTMROC00 packaged in plastic TQFP packages. Essentially all of these have now been passed through production level tests at Penn and the measured yields are as follows:

493 chips in the Data Base

186 pass all digital tests (38%)

2 of these fail DAC extrema test

22 of these fail step size test

162 pass digital AND DAC (33%)

473 pass DAC maxima test (96%)

221 pass TP test (45%)

test details:

fail TEST % fail

------ --------------- ------

67 RWconfig (14%)

63 RWthresh1 (13%)

63 RWthresh2 (13%)

66 RWtpconf (13%)

60 RWtpdelay (13%)

69 RWtm (14%)

493 Pipeline **** (100%)

190 Derandomizer (39%)

157 HighPulse (32%)

143 Address (29%)

42 ALL (9%)

**** Note that the Pipeline test is not yet operational for the 00 version and so this number is meaningless (we need to run a converted Verilog "expected vectors" file through the IMS conversion routine to get correct "expected" vectors into the IMS tester. However, the Derandomizer test covers essentially the same territory and in the 99 version of the chip the correlation was 100% except that the Pipeline test covers the L1ID and BCID counters which are NOT covered by the Derandomizer test - failures in those counters were very rare in the previous version, but we need to add that in and then retest the lot in order to get an accurate accounting.

This 33% yield is very similar to the old version yield increased by the improvement in the DAC circuitry, the high failure rate in the Address test continues to be puzzling as that circuitry is quite simple. Otherwise, things are as expected and we have a reasonable basis on which to estimate costs - unfortunately there were no magic increases in yield.

1.2.5.3 PCB – End Cap

1.2.5.3.1 Design — Richard Van Berg (University Of Pennsylvania)

The present ASD Stack and DTM Triple Flex board designs are being modified to use the ASDBLR/DTMROC00 pinouts - these are very small changes except that one control line (shaper select) has to be routed through the between board connectors - a single ground pin will be sacrificed. The new boards will be used for system and radiation tests - they are expected to perform as well as the previous versions since the changes are minor.

1.2.5.3.2 Prototype — Richard Van Berg (University Of Pennsylvania)

Additional measurements at CERN continue to indicate good behavior for the present design. The sector prototype was run in the GIF facility at CERN with a background gamma flux simulating a reasonable fraction of the final LHC flux and performance was as expected. The next set of tests are divided into system tests and radiation tests using End Cap boards with new (00) chips. This includes neutron, proton, and gamma irradiation and a high rate test at the Weizman Institute where the background flux can be made significantly larger than full LHC levels. All this work is being carried out at CERN.

1.2.5.5 Beam Test

Milestone	Baseline	Previous	Forecast	Status
End of 01 Test Beam	28-Sep-01	--	4-Nov-01	Delayed (See #1)

Note #1 We have been granted additional time up through Nov. 4 01. This is a GOOD thing.

Richard Van Berg (University Of Pennsylvania)

The test beam is proceeding nicely. A TB3 board with a calibrated ASDBLR00 on was delivered in late July and is being used for single straw high rate tests. The DAQ software is running well, Kristian Hahn is presently in residence at CERN seeing to support. The effort to get the sector prototype running in the beam this year may have problems because of difficulty in getting revised versions of the Endcap boards fabricated soon enough - still we do have until early November - so all hope is not yet abandoned.

1.2.5.6 System Integration & Installation

Milestone	Baseline	Previous	Forecast	Status
System Design Certified	1-Oct-01	--	1-Oct-01	On Schedule (See #1)

Note #1 Well, hmmm, this depends upon getting large enough system tests in place before Oct. and that needs not only the chips (which we now have) but also End Cap boards (which CERN is having difficulty getting) so 1 Oct may be too tight. It is certainly beyond reason to expect that the Barrel will be in good shape on this time scale - but see the System Integration section.

Richard Van Berg (University Of Pennsylvania)

The End Cap System Integration is taking place almost entirely at CERN and was covered under End Cap Board Design and Prototyping. The Barrel System Integration is taking place at Penn and is covered here.

Last month we received ten stamp flex boards from Lund with ASDBLR99 die wire bonded (but not protected). We have glop topped these, added DTMROC chips and tested the boards. Three of them work perfectly and several of the others work to a large degree (i.e. have one or a few bad channels or fail a non-critical digital test). We also received two sets of Module 2 snake cables from Lund. We have installed connectors on the snake cables and demonstrated at the one and two stamp level that the cable works well.

However, we have also shown that the design of the stamp boards introduces unacceptable levels of pickup in the ASDBLR inputs so that most of the channels on a board need to have thresholds set above 5fC (way above our desired 1.5-2 fC threshold) to keep the output rates at any reasonable level - this is WITHOUT the chamber installed - that is almost certain to make matters worse. So, until we have FBGA packages and stamp boards (the topology is such as to obviate the crossing of inputs and outputs necessary in the present design) we cannot proceed very far on tests sensitive to actual noise levels. Still, there are many areas that need testing ranging from simply being able to power about a dozen stamp boards on one snake to cooling, signal transmission, addressing, etc.

Unfortunately, the TTC module developed a fault recently and that must be repaired before we can move beyond the two stamp level - presumably a driver chip failed, but as the TTC was "protected" by an intermediate active patch panel we also need to clarify the failure mode and feed that back to the next version TTC design.

1.3 ARGON

Milestones with changed forecast dates:

1.3.1.5 Assembly & test in West Hall

Milestone	Baseline	Previous	Forecast	Status
Final Kryostat Acceptance (KHI-CERN)	31-Aug-01	31-Aug-01	31-Dec-01	See Note #1

Note #1 Provisional acceptance and transfer of ownership to CERN completed. Final acceptance awaits completion of chimney weld repair.

1.3.2.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
Last Pin Carrier Delivery	1-Mar-01	1-Sep-01	1-Dec-01	Delayed (See #1)

Note #1 After initial delay, the production matches the new ATLAS schedule

1.3.2.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
Barrel FTs (Mechanical) Delivered to CERN	1-May-01	20-Aug-01	20-Oct-01	Delayed (See #1)
Barrel FTs (Electrical) delivered to CERN	1-Jun-01	15-Sep-01	15-Feb-02	Delayed (See #2)

Note #1-2 The delivery will match the installation program.

1.3.2.2.4 Installation

Milestone	Baseline	Previous	Forecast	Status
Ship End-Cap C to CERN	5-Mar-01	20-Aug-01	20-Oct-01	Delayed (See #1)
Installation HVFT on Endcap C complete (mechanical)	1-Nov-01	1-Nov-01	20-Jan-02	Delayed (See #2)

Note #1 Shipment combined with signal FT.
Note #2 Delay will match the cryostat availability.
The order of installation of HV and signal FT has been changed. HV cables will be installed after completion of signal FT installation.

1.3.3.1.2 LN2 Ref. System Procurement

Milestone	Baseline	Previous	Forecast	Status
Start Production	1-Aug-01	3-Sep-01	15-Sep-01	Delayed (See #1)

Note #1 The order to start production will be placed in September.

1.3.3.1.3 LN2 Ref. System Fabrication

Milestone	Baseline	Previous	Forecast	Status
LN2 Ref. System Fabrication Start	1-Jun-01	20-Aug-01	15-Sep-01	Delayed (See #1)

Note #1 The order to start fabrication will be placed in September.

1.3.3.2.2 Quality Meter Prototype

Milestone	Baseline	Previous	Forecast	Status
Quality Meter Prototype	1-May-00	21-Aug-01	21-Sep-01	Delayed (See #1)

Note #1 The prototype exists. An improved design with higher reliability is under development and will be tested in September.

1.3.4.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
Last Delivery of SB & MB PC Boards	1-Dec-01	1-Feb-02	1-Nov-02	Delayed (See #1)

Note #1 Vendor quality problems that have now been resolved.

1.3.5.1.3 Production (QTY=30000)

Milestone	Baseline	Previous	Forecast	Status
Start Preamp Deliveries to FEB	3-Sep-01	3-Sep-01	1-Apr-02	Delayed (See #1)

Note #1 BNL is holding completed Preamps until FEB requests them. To date, 10,144 have been completed and ready for shipment.

1.3.7.1.2 Pre-Proto/Mod 0/Atlas Prototype

Milestone	Baseline	Previous	Forecast	Status
Rad Tol. FEB Design Review	1-May-01	3-Sep-01	24-Oct-01	Delayed (See #1)
Critical Design Review	3-Sep-01	3-Sep-01	24-Oct-01	Delayed (See #2)
Start Assembly	11-Sep-01	11-Sep-01	11-Nov-01	Delayed (See #3)

Note #1 Delayed due to late delivery of rad-tol voltage regulators.
Note #2 Delayed due to scheduling conflicts with the reviewers.
Note #3 Delayed due to the delay in the Critical Design Review.

1.3.8.2.1 Design/Electronic Tooling/Comp. Specs

Milestone	Baseline	Previous	Forecast	Status
Circuit Design of ATLAS receiver Complete	12-Aug-01	12-Sep-01	12-Oct-01	Delayed (See #1)
Final Design Complete	4-Oct-01	4-Oct-01	4-Dec-01	Delayed (See #2)
Critical Design Review	12-Dec-01	12-Dec-01	12-Feb-02	Delayed (See #3)

Note #1 The choice for the variable gain amplifier IC for the receiver is being revisited. We have found a promising candidate, a 10-bit multiplying DAC with 70 MHz bandwidth and have successfully passed our pulse through it, observing essentially no distortion. We are now building a more complete prototype circuit for final tests.
Note #2 It is likely that this milestone will be missed by a few months, due to the delay arising from the study of the variable gain amplifier mentioned above.
Note #3 This milestone has slipped, since the production of the prototype module is delayed.

1.3.9.1.1 Design

Milestone	Baseline	Previous	Forecast	Status

Complete Code to form averages of Cal.	18-Jun-01	1-Sep-01	1-Nov-01	Delayed (See #1)
Complete Code to get OFC from CAL. Data	4-Sep-01	4-Sep-01	1-Nov-01	Delayed (See #2)

Note #1 -2 Calibration procedure not completely defined.

1.3.10.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
FCAL1-C Interconnects Complete	30-Apr-01	30-Sep-01	30-Nov-01	Delayed (See #1)
FCAL1-C Tube Swaging Complete	1-Oct-01	31-Aug-01	30-Sep-01	Delayed (See #2)
Delivery 1st half - FCAL1-A	3-Dec-01	3-Dec-01	31-Aug-01	Completed (See #3)

Note #1 The order for the interconnect boards has been placed. Because we are doing both FCal1C and FCal1A interconnects at the same time, each step is taking a bit longer. The anticipated additional delay is not on the critical path and therefore not a concern.
Note #2 As explained in the written report our swaging gun (tool) fails after several swages. We are trying new, more robust parts. If this works ok then we are planning to implement a second crew to try to make up some of the lost time.
Note #3 As noted in the written report, eleven absorber plates arrived during the last week of August.

1.3.1 Barrel Cryostat

1.3.1.5 Assembly & Test in West Hall

Milestone	Baseline	Previous	Forecast	Status
Final Kryostat Acceptance (KHI-CERN)	31-Aug-01	31-Aug-01	31-Dec-01	See Note #1
Calorimeter Support Structure Complete	31-Oct-01	--	31-Oct-01	On Schedule

Note #1 Provisional acceptance and transfer of ownership to CERN completed. Final acceptance awaits completion of chimney weld repair.

Barrel Cryostat Monthly Report **Jack Sondericker (Brookhaven National Lab.)**

The last sentence of the July Barrel Cryostat Report said; presently, discussions are on going with Kawasaki, CERN and BNL to come to agreement on how best carry out the (chimney weld) repair. By mid August, after X raying the weld and more discussion, repair was not on a path of convergence. Furthermore, the cryostat installation schedule was being pressed so BNL undertook to set into motion an agreement whereby CERN would accept the Barrel Cryostat with the provision that the chimney weld be repaired, at a slightly later time, to Specification standards.

The last document was signed on August 28th and the title of the Barrel Cryostat was provisionally transferred from Kawasaki to Brookhaven and on to CERN. This maneuver gives CERN the legal right to start to remove bulkheads and preparation for installation work.

Discussions continue on the process of weld repair.

1.3.2 Feedthrough

1.3.2.1 FT-Signal

1.3.2.1.1 Design

Milestone	Baseline	Previous	Forecast	Status
I/F Equipment Avail for Final Cryostat Complete	3-Sep-01	--	3-Sep-01	On Schedule

1.3.2.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
Last Pin Carrier Delivery	1-Mar-01	1-Sep-01	1-Dec-01	Delayed (See #1)
34 FT Complete	15-Oct-01	--	15-Oct-01	On Schedule (See #2)
54 FT Complete	17-Dec-01	--	17-Dec-01	On Schedule

Note #1 After initial delay, the production matches the new ATLAS schedule

Note #2 34 FT completed on 10-Sep-01.

Bob Hackenburg (Brookhaven National Lab.)

August saw the total feedthrough count rise to 34, with the 1st four feedthroughs arriving at CERN, B180, in excellent condition. We are still awaiting completion in B180 of the fenced-in area to store the FTs, and the FT electrical testing workshop. The procedures for the "painting" (i.e., the Oakite) of the cryostat are all cleared, and we are waiting for the chemicals themselves to arrive at CERN. Dave Pate, BNL's new man at CERN, arrived in mid-August and has been hard at work preparing everything for the Oakite "painting" and the FT installation. The new tester is ready for shipment to CERN, and we are finalizing our documentation on it, and expect to ship it by Sept. 12, via air.

1.3.2.1.4 Installation

Milestone	Baseline	Previous	Forecast	Status
Installation	17-Jan-01	--	30-Sep-02	Delayed (See #1)
Start Installation Procedure	13-Jul-01	--	15-Sep-01	Delayed (See #2)
Last Shipment	31-Oct-01	--	30-Aug-02	Delayed (See #3)

Note #1 The completion date matches new ATLAS schedule.

Note #2 Installation cannot start before the acceptance tests of the cryostat are complete.

Note #3 The last shipment date matches the new ATLAS schedule. Feedthroughs production will be completed earlier.

1.3.2.2 HV Feedthrough

1.3.2.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
2 Complete HV Feedthrough Ports	1-Mar-01	--	20-Jan-02	Delayed (See #1)
Barrel FTs (Mechanical) Delivered to CERN	1-May-01	20-Aug-01	20-Oct-01	Delayed (See #2)
Barrel FTs (Electrical) delivered to CERN	1-Jun-01	15-Sep-01	15-Feb-02	Delayed (See #3)
Production Complete	14-Sep-01	--	20-Jan-02	Delayed (See #4)

Note #1 The order of installation of HV and signal FT has been changed. HV cables will be installed after completion of signal FT installation

Note #2-3 The delivery will match the installation program

Note #4 The order of installation of HV and signal FT has been changed. HV cables will be installed after completion of signal FT installation

1.3.2.2.4 Installation

Milestone	Baseline	Previous	Forecast	Status
Ship End-Cap C to CERN	5-Mar-01	20-Aug-01	20-Oct-01	Delayed (See #1)
Ship Barrel to CERN	1-May-01	--	20-Aug-01	Completed
Installation HVFT ports on Endcap C	5-Sep-01	--	25-Nov-01	Delayed (See #2)
Barrel Install Complete	1-Nov-01	--	20-Jan-02	Delayed (See #3)
Installation HVFT on Endcap C complete (mechanical)	1-Nov-01	1-Nov-01	20-Jan-02	Delayed (See #4)

Note #1 Shipment combined with signal FT.

Note #2, 4 Delay will match the cryostat availability.

Note #3 The order of installation of HV and signal FT has been changed. HV cables will be installed after completion of signal FT installation.

The order of installation of HV and signal FT has been changed. HV cables will be installed after completion of signal FT installation

1.3.3 LAr Cryogenics

1.3.3.1 LN2 Refrigerator System

1.3.3.1.2 LN2 Ref. System Procurement

Milestone	Baseline	Previous	Forecast	Status
Proposal Assessment & Contract Start	1-Feb-01	--	20-Aug-01	Completed
LN2 Ref.System Procurement Complete	2-Apr-01	--	20-Aug-01	Completed
Start Production	1-Aug-01	3-Sep-01	15-Sep-01	Delayed (See #1)

Note #1 The order to start production will be placed in September.

LN2 Refrigerator Procurement **Jack Sondericker (Brookhaven National Lab.)**

Placement of the order for the LN2 refrigerator moved ahead at a slow pace due to asynchronous vacations of all parties concerned. Announcement of placement of the order should be made in the first week of September.

1.3.3.1.3 LN2 Ref. System Fabrication

Milestone	Baseline	Previous	Forecast	Status
Ln2 Ref. System Fabrication	1-Jun-01	--	1-Sep-03	Delayed (See #1)
LN2 Ref. System Fabrication Start	1-Jun-01	20-Aug-01	15-Sep-01	Delayed (See #2)

Note #1 The completion date of system installation matches new ATLAS installation schedule.

Note #2 The order to start fabrication will be placed in September.

1.3.3.2 LN2 Quality Meter System

1.3.3.2.2 Quality Meter Prototype

Milestone	Baseline	Previous	Forecast	Status
Quality Meter Prototype	1-May-00	21-Aug-01	21-Sep-01	Delayed (See #1)
Final Design Review	1-May-01	--	15-Dec-01	Delayed (See #2)
Specification PRR Review	1-Aug-01	--	15-Dec-01	Delayed (See #3)

Note #1 The prototype exist. An improved design with higher reliability is under development and will be tested in September.

Note #2 Will match the cryostat installation schedule.

Note #3 The prototype exist. An improved design with higher reliability is under development.

Quality Meter Prototype **Jack Sondericker (Brookhaven National Lab.)**

The electronic circuit board was delivered, as promised, on the first of the month. After a week of board stuffing and debugging, initial tests were carried out. Early data indicates that the capacitance measuring circuitry is very stable and has resolution that exceeds requirements. Method of canceling distributed capacitance of very long leads between sensor and board have proven to be a complete success.

Mechanical pieces of the prototype are in the shops being machined and welded to prints. Cold testing of the prototype will take place in September.

1.3.3.2.3 Quality Meter Production

Milestone	Baseline	Previous	Forecast	Status
Parts and Material Start	29-Aug-01	--	15-Jan-02	Delayed (See #1)
Quality Meter Production	1-Oct-01	--	30-Jun-02	Delayed (See #2)
Assembly Start	26-Dec-01	--	26-Jun-02	Delayed (See #3)
Machining and Welding Start	26-Dec-01	--	26-Jun-02	Delayed (See #4)
Tests and calibration Start	26-Dec-01	--	26-Dec-02	Delayed (See #5)
Parts and Material Complete	28-Dec-01	--	28-Aug-02	Delayed (See #6)

Note #1, 3-6 Delay matches the new ATLAS schedule. Not on critical path.

Note #2 Delay matches the new ATLAS schedule.

1.3.4 EM Electronics/MB System

1.3.4.2 Motherboard System

1.3.4.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
Delivery of Module 5 boards	1-Jun-01	--	1-Jun-01	Completed (See #1)
Delivery of Module 6 boards	20-Jun-01	--	20-Jun-01	Completed (See #2)
Delivery of Module 7 boards	15-Jul-01	--	20-Aug-01	Completed (See #3)
25% MB System Production Complete	6-Aug-01	--	31-Aug-01	Completed (See #4)
Delivery of Module 8 boards	1-Sep-01	--	1-Sep-01	On Schedule (See #5)
Delivery of Module 9 mother boards	14-Sep-01	[New]	14-Sep-01	On Schedule (See #6)
Delivery of Module 10 boards	30-Sep-01	[New]	30-Sep-01	On Schedule

Last Delivery of SB & MB PC Boards	1-Dec-01	1-Feb-02	1-Nov-02	Delayed (See #7)
50% MB System Production Complete	2-Dec-01	--	2-Dec-01	On Schedule

Note #1 Shipped to Saclay on May 31, 2001.

Note #2 Shipped to Annecy on July 11, 2001.

Note #3 Shipped to Annecy on Aug. 24, 2001.

Note #4 Completed on 24-Aug with delivery of 8 module kits.

Note #5 Shipped to CERN on August 24, 2001.

Note #6 Shipped to CERN on August 31, 2001.

Note #7 Vendor quality problems that have now been resolved.

Srini Rajagopalan (Brookhaven National Lab.)

Batch 7: completed, packed, shipped to Annecy on August 24, 2001

Batch 8: completed, packed, shipped to CERN on August 24, 2001

Batch 9: completed, packed, shipped to Saclay on August 31, 2001

Summing Boards: Most boards received, and being inspected.

High Voltage Board: Most Boards received, inspected and in test.

Front Mother Boards: Most boards received, inspected, and in test.

Back Mother Boards: Most boards received, inspected, and in test.

Alignment Boards: In stock at BNL.

A new protection network scheme for the calibration resistive network on the motherboards was proposed by BNL at the August 28 EMB group rep meeting at CERN. BNL has developed and tested several add on boards and demonstrated its ability to protect the calibration resistive networks against accidental electrostatic discharges. At the Aug 28, meeting, it was decided that BNL develop sufficient number of prototypes that can be tested at CERN testbeam. BNL has proceeded to develop these prototype protective boards which will be delivered to CERN for tests in September.

The protective boards utilize a BAV70 protection diode (the same that is used in the preamplifiers) together with a 10 ohm series resistance. Apart from its ability to protect against electrostatic discharges, we are also investigating its radiation hardness and comparing them with other diodes successfully used in high radiation environment. A final decision on these protective networks is expected during the LAr week in October.

1.3.5 Preamp/Calibration

1.3.5.1 Preamps

1.3.5.1.3 Production (QTY=30000)

Milestone	Baseline	Previous	Forecast	Status
Start Preamp Deliveries to FEB	3-Sep-01	3-Sep-01	1-Apr-02	Delayed (See #1)

Note #1 BNL is holding completed Preamps until FEB requests them. To date, 10,144 have been completed and ready for shipment.

Hong Ma (Brookhaven National Lab.)

IO-826: received 864 from vendor since last report. All except 96 have been tested. Total: 2880 have been completed and ready for shipment. Average yield = 97.2%

IO-824: Received 1056 from vendor this month. All are being tested. Total: 2208 have been completed and ready for shipment. Average yield 98.9%

IO-823: Received none from vendor since last report. Total: 5056 have been completed and ready for shipment. Average yield 99.3%

1.3.6 System Integration

1.3.6.1 Pedestal

1.3.6.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
Start Barrel Pedestal Delivery to CERN	31-Dec-01	--	31-Dec-01	On Schedule
Start EC Pedestal Delivery to CERN	31-Dec-01	--	31-Dec-01	On Schedule
Start Ped.s deliveries Ship In Place	31-Dec-01	--	31-Dec-01	On Schedule
25% Pedestals Delivery from Vendor Compl	30-Jan-02	--	30-Jan-02	On Schedule

1.3.6.2 Cables/Base Plane

1.3.6.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
80% Warm Cables Delivered	28-Dec-01	--	28-Dec-01	On Schedule
80% Warm Cables Ship in Place	28-Dec-01	--	28-Dec-01	On Schedule
10% Deliveries Complete	31-Dec-01	--	31-Dec-01	On Schedule
10% Deliveries Ship in Place	31-Dec-01	--	31-Dec-01	On Schedule
1st Delivery Date to CERN	31-Dec-01	--	31-Dec-01	On Schedule
1st Delivery Ship in Place	31-Dec-01	--	31-Dec-01	On Schedule

1.3.6.3 Crate-Mechanical

1.3.6.3.3 Production

Milestone	Baseline	Previous	Forecast	Status
25% Crates Deliveries from Vendor Compl	30-Jan-02	--	30-Jan-02	On Schedule

1.3.6.4 Power and Services

1.3.6.4.3 Production

Milestone	Baseline	Previous	Forecast	Status
25% Bus Bars Delivered from Vendor	30-Jan-02	--	30-Jan-02	On Schedule

1.3.6.5 Cooling

1.3.6.5.3 Production

Milestone	Baseline	Previous	Forecast	Status
Cooling Liquid Decision	17-Dec-01	--	17-Dec-01	On Schedule

1.3.7 Front End Board

1.3.7.1 FEB

1.3.7.1.1 Design — John Parsons (Columbia University)

The design and layout of the FEB has been completed. Detailed checking will proceed in September, with the aim to be ready to produce the first board during October.

We continue studies of possible Voltage regulator backups. We have identified one commercial regulator which meets our specs, but is prohibitively expensive. Our focus, therefore, is now on producing regulators using discrete commercial components. We continue our radiation testing of possible components (see report below).

1.3.7.1.2 Pre-Proto/Mod 0/Atlas Prototype

Milestone	Baseline	Previous	Forecast	Status
Freeze Component for ATLAS Prototype	1-Mar-01	--	1-Aug-01	Completed
Freeze Connector Location	1-May-01	--	1-Sep-01	Delayed (See #1)
Rad Tol. FEB Design Review	1-May-01	3-Sep-01	24-Oct-01	Delayed (See #2)
1st Delivery of Layer Sum Boards	2-Jul-01	--	1-Jan-02	Delayed (See #3)
Feb - ATLAS Layout Complete	21-Aug-01	--	21-Aug-01	Completed
Critical Design Review	3-Sep-01	3-Sep-01	24-Oct-01	Delayed (See #4)
Start Assembly	11-Sep-01	11-Sep-01	11-Nov-01	Delayed (See #5)
Rad Hard. - All Components	28-Sep-01	--	28-Feb-02	Delayed (See #6)
Final Dec. DMILL/IBM	7-Dec-01	--	7-Dec-01	On Schedule

Note #1 Delayed due to delay in finalizing TTC connector.

Note #2, 6 Delayed due to late delivery of rad-tol voltage regulators.

Note #3 Delayed until boards are needed for rad-tol FEB production.

Note #4 Delayed due to scheduling conflicts with the reviewers.

Note #5 Delayed due to the delay in the Critical Design Review.

1.3.7.1.5 Radiation Testing **John Parsons (Columbia University)**

We performed additional p-irradiation tests at Harvard the weekend of Aug. 18/19. Part of the time was spent, with SMU, irradiating the new optical transmitter from Taiwan for the optical link; it was seen that the part died from the irradiation and is not yet suitable for use in ATLAS.

In addition, we irradiated NMOS devices for possible use as pass transistors in voltage regulator design. All devices showed threshold voltage shifts with dose, though some might be usable in ATLAS. Further analysis of the data is on-going.

We have booked Harvard again for Sept. 8/9. We plan to irradiate samples of the DSM CLKFO chip, as well as additional pass transistor candidates.

1.3.7.2 SCA

1.3.7.2.1 Design — John Parsons (Columbia University)

A 3-day meeting was held on Aug. 21-23 at Nevis, where D. Breton (LAL) presented their test results for the SCA chips from the first 6 wafers of the engineering run. A discussion was held about where to place the selection cuts defining acceptable chips. The estimated yield is about 65%.

Meetings are being scheduled with ATMEL for Oct. and Dec. to serve as the PRR to allow production to proceed. Before those meetings, we must still:

1. Finalize the acceptance cuts (Nevis, Orsay, Saclay).

2. Test the SCA chips from the remaining two eng. run wafers (Orsay, Saclay, Grenoble).

3. Perform tests of eng. run chips on a Module 0 FEB (Nevis).

1.3.7.4 Optical Links

1.3.7.4.1 Design — John Parsons (Columbia University)

Discussions with Taiwan after the poor irradiation results revealed that they had not in fact used all the same components as the previously qualified Methode transceiver. The transmitter will be redesigned with the correct components, at which point further irrad. tests will be performed.

The PRR for the optical link has been scheduled for December.

1.3.7.4.2 Prototype/Module 0

Milestone	Baseline	Previous	Forecast	Status
Optical Links ATLAS Prototype	1-Jun-01	--	1-Jun-02	Delayed (See #1)

Note #1 Prototype completed and tested. FEB-end integrated with the layout. ROD-end will depend on the ROD design.

1.3.8 Trigger Summation

1.3.8.1 Layer Sums

1.3.8.1.3 Production (Qty = 3,441 Boards)

Milestone	Baseline	Previous	Forecast	Status
Start Deliveries to FEB (ORSAY/Nevis)	2-Jul-01	--	1-Jan-02	Delayed (See #1)

Note #1 Delivery will be started to Nevis or Orsay only when requested.

Bill Cleland (University Of Pittsburgh)

In August, we have completed the functionality tests of all of the LSBs received from the assembler. We are now finishing the burn-in and detailed tests, which take somewhat longer (burn-in for 1 week is the bottleneck).

We have reworked all of the S1x16 boards and S2x8 boards which failed at some point in the testing (roughly 3%), and all are now operational. The rework on the G=2 S1x16 boards to add a resistor to ground and make a small compensating adjustment to the gain has started. At the request of Nevis, we are looking into the feasibility of adjusting the operating voltages for the LSBs in an effort to reduce the number of voltage regulators.

1.3.8.2 Interface to Level 1

1.3.8.2.1 Design/Electronic Tooling/Comp. Specs

Milestone	Baseline	Previous	Forecast	Status
Circuit Design of ATLAS receiver Complete	12-Aug-01	12-Sep-01	12-Oct-01	Delayed (See #1)
Final Design Complete	4-Oct-01	4-Oct-01	4-Dec-01	Delayed (See #2)
Critical Design Review	12-Dec-01	12-Dec-01	12-Feb-02	Delayed (See #3)

Note #1 The choice for the variable gain amplifier IC for the receiver is being revisited. We have found a promising candidate, a 10-bit multiplying DAC with 70 MHz bandwidth and have successfully passed our pulse through it, observing essentially no distortion. We are now building a more complete prototype circuit for final tests.

Note #2 It is likely that this milestone will be missed by a few months, due to the delay arising from the study of the variable gain amplifier mentioned above.

Note #3 This milestone has slipped, since the production of the prototype module is delayed.

Bill Cleland (University Of Pittsburgh)

In August we have completed the prototype boards making up the receiver chain, and all except the variable gain amplifier (VGA) have been tested for functionality. For the VGA we have evaluated two multiplying DACS. One was eliminated due to its limited bandwidth, but the other looks quite promising. We now need to build a prototype board which tests it in the configuration we plan to use for the VGA. Finally, the FPGA for the control logic has been completed. We are now in the process of modifying it to accommodate the new version of SPAC.

1.3.9 ROD System

1.3.9.1 ROD Board

1.3.9.1.1 Design

Milestone	Baseline	Previous	Forecast	Status
Reconstruct E, T, and chisquare for TB data	12-Feb-01	--	1-Nov-01	Delayed (See #1)
Complete Code to form averages of Cal.	18-Jun-01	1-Sep-01	1-Nov-01	Delayed (See #2)
Complete Code to get OFC from CAL. Data	4-Sep-01	4-Sep-01	1-Nov-01	Delayed (See #3)
Real time evaluation of optimal filter coeff.	3-Dec-01	--	3-Dec-01	On Schedule
Conceptual Design Reivew	15-Jan-02	--	15-Jan-02	On Schedule
Conceptual Design Reivew	15-Jan-02	--	15-Jan-02	On Schedule

Note #1 Done, not completely reviewed

Note #2-3 Calibration procedure not completely defined

1.3.9.1.2 Prototype

Milestone	Baseline	Previous	Forecast	Status
Decision Taken on Processor Hardware	10-Dec-01	--	10-Dec-01	On Schedule

1.3.10 Forward Calorimeter

1.3.10.1 FCAL1 Module

1.3.10.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
FCAL1-C Interconnects Complete	30-Apr-01	30-Sep-01	30-Nov-01	Delayed (See #1)
FCAL1-C Tube Swaging Complete	1-Oct-01	31-Aug-01	30-Sep-01	Delayed (See #2)
Delivery 1st half - FCAL1-A	3-Dec-01	3-Dec-01	31-Aug-01	Completed (See #3)
FCAL1-A Matrix Plate Inspection-1	10-Dec-01	--	10-Dec-01	On Schedule (See #4)

Note #1 The order for the interconnect boards has been placed. Because we are doing both FCal1C and FCal1A interconnects at the same time, each step is taking a bit longer. The anticipated additional delay is not on the critical path and therefore not a concern.

Note #2 As explained in the written report our swaging gun (tool) fails after several swages. We are trying new, more robust parts. If this works ok then we are planning to implement a second crew to try to make up some of the lost time.

Note #3 As noted in the written report, eleven absorber plates arrived during the last week of August.

Note #4 The plates that just arrived will probably sit in storage awaiting completion of the copper rod cleaning before we QC them. This may start in October.

FCal1 Module **John Rutherfoord (University Of Arizona)**

The LHCC Comprehensive Review was held in early July and one of the issues the reviewers flagged was the lateness of the FCal Calibration test beam run. It is presently scheduled to begin late in August of 2003. They worry that if the FCal schedule were to slip by just a bit (which is not unlikely due to the still large uncertainties in the tungsten rod delivery schedule) then this test might be pushed off the end of the CERN accelerator schedule for 2003 and into 2004, which is too late.

(The LHCC also reiterated their view of the importance of what we now call the crack studies, presently scheduled for summer 2004. This was formerly called the combined EMEC/HEC/FCal test beam run whose goal is to scan the transition between these calorimeter systems.)

As a result, the ATLAS EB asked Horst and Horst asked us what it would take to advance our schedule so that this important calibration test could be started in early June of 2003, approximately three months sooner than planned. Horst gave us until the beginning of September (i.e. now) to respond. The FCal community discussed this question several times and iterated its draft of a written response to Horst. In short, we told Horst that it might be possible to advance our schedule by three months if funds could be found to purchase most of the FCal2A and FCal3A tungsten rods with orders placed early this Fall. (Russian funding difficulties forced ITEP to renege on their commitment for FCal3A rods and their funds for the FCal2A rods won't arrive until sometime in 2002. Our colleagues in China hope to pick up some of the Russian commitment but it seems unlikely that their funding agency will reach a decision soon enough.)

We also pointed out that each of the three production sites would have to overlap production of their C modules with their A modules, requiring another team of people and with a certain inefficiency due to space limitations and stretching of the management.

In particular, we at Arizona have analyzed our production capabilities and find that with no float in our schedule (due to the long delay in the approval of a copper matrix plate machining contract), the required upgrade of our resources during this overlap period is probably not just a simple scaling from our present resources. We have requested some help from the US ATLAS Project Office in carefully and accurately accessing our needs.

We expected to start swaging the copper electrode tubes at the start of this reporting period. However the swaging tool was not ready on time and, when it was ready, it failed. This was a surprise to us since it is the same tool we used on our Module 0 and it worked without mishap. We are now trying more robust parts hoping to find a reliable solution. According to our schedule we should have completed the swaging at the end of this reporting period but only about 3% is done. We are discussing the possibility of training another team (2 people per team) so that swaging can be done throughout the day, allowing us to catch up a bit.

In the meantime drilling the holes for the signal pins in the copper electrode rods continues with about 97% of all rods (for both modules) completed. About 87% of these rods have been cleaned but only 25% have been inspected. This is because our expert team of students were recently out of commission due to the start of classes. They are scheduled to start up their usual work pattern next week after which we expect to catch up quickly in this QC step.

Some (~5%) of the pin holes in the copper rods were observed to be either off center or miss-aligned with the rod axis (or both). These will be returned to the shop where a better quality hole will be drilled in the other end.

Eleven FCal1A copper absorber plates arrived from the Science and Technology Center (STC) at Carleton University (the machine shop producing our matrix) during the last week of August. The shop is on schedule to complete this job by the contract date of 26 October. However we have requested two changes which will throw them off their schedule so we are presently negotiating a new schedule. We expect to receive the remainder of the absorber plates by the present due date but receive the two end plates on a new schedule (if this is the optimal scheme to effect the change).

In any event our present schedule shows us cleaning these absorber plates right up until the expected new delivery date of the end plates so this will not throw off even our accelerated schedule discussed above.

1.3.10.2 FCAL Electronics

1.3.10.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
PCBs received at AZ	21-Nov-00	--	15-Dec-01	Delayed (See #1)

Note #1 The order for a sample PCB is out to the winning bidder. This sample should arrive in September and be acceptance checked.

Cold Electronics **John Rutherfoord (University Of Arizona)**

All of the second half of the shipment of Axon cold cables, which arrived in July, have been acceptance tested, as described last month, and passed.

We sent several of the pre-production evaluation transmission line transformers to Sergio Rescia at BNL to check for frequency response warm and cold. Sergio just returned from vacation last week and promised to jump on this later in his first week back. We hope to hear the results of his tests early in this coming week. Once we tell the production house to proceed, they can produce about 500 transformers per week. We need a total of 4000 transformers including spares.

1.4 TILE

Milestones with changed forecast dates:

1.4.3.3.3 Production

Milestone	Baseline	Previous	Forecast	Status

MB Card Test 25% Complete	1-May-01	1-Oct-01	1-Dec-01	Delayed (See #1)
MB Card Test 50% Complete	1-Aug-01	30-Nov-01	1-Feb-02	Delayed (See #2)
MB Card Test 100% Complete	24-Dec-01	24-Dec-01	1-Jun-02	Delayed (See #3)

Note #1-3 On track for current forecast and not on critical path.

1.4.4.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
Ship submodules 41-44 to ANL	27-Aug-01	27-Aug-01	27-Oct-01	Delayed (See #1)

Note #1 Due to delayed startup of production in 1999, we are 2 months behind original schedule. There is no impact on module production.

1.4.4.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
Start Scintillator Assembly	7-Sep-01	7-Sep-01	1-Nov-01	Delayed (See #1)

Note #1 Purchase of the mechanical components for the crack scintillators is awaiting final checks by the ATLAS technical coordination team.

1.4.1 Extended Barrel Mechanics **James Proudfoot (Argonne National Lab.)**

Good progress was achieved in all areas in August. Submodule production is complete at the University of Chicago. A total of 175 submodules have been completed at ANL, where in addition, repairs were completed on 4 of the problem UC submodules. 175 submodules have been completed at the University of Illinois, of which 168 have been shipped to Argonne. Final drawings for the special, cut submodules are being drawn up and we expect to review these and approve them for construction in the October Atlas meeting. 40 modules have been mechanically completed of which 32 have been instrumented, tested and shipped to CERN. All modules are meeting both the mechanical and optical specification. 2 additional modules are in the final stages of instrumentation and should be completed in September. Documentation of the extensive design and engineering analysis associated with the design of the extended barrel support saddle has been completed in preparation for an engineering meeting to be held in September. A small number of issues have been identified and will discussed and hopefully resolved at this meeting.

1.4.1.1 Submodules
1.4.1.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
Submodule Completion (509 Cum)	14-Dec-01	--	14-Dec-01	On Schedule

Victor Guarino (Argonne National Lab.)

During the month of August six submodules were constructed and are ready for mounting in a module. Four additional submodules were stacked and welded but were not inspected or painted. Four UC submodules were also dismantled because of problems with their slots and restacked. They need final painting.

Steven Errede (University Illinois-Urbana-Champaign)

In August 2001, we again made 11 ATLAS TileCal submodules. We have now made a total of 175 submodules (only 17 more to go!) We shipped a full batch of 16 TileCal submodules to Argonne in ~ mid-August. A total of 168 submodules have now been shipped to Argonne from UIUC.

1.4.1.2 Extended Barrel Module
1.4.1.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
Last Delivery of Girders	21-Dec-01	--	21-Dec-01	On Schedule
Module Completion (50 Cum)	31-Jan-02	--	31-Jan-02	On Schedule
Modules Shipped to CERN (40 Cum)	31-Jan-02	--	31-Jan-02	On Schedule

Victor Guarino (Argonne National Lab.)

ANL modules #39, 40, and 41 were constructed during the month of August. No problems were encountered during their construction. In addition, four modules were shipped to CERN.

ANL is preparing for the construction of the special modules. The drawings for the special submodules that go into these modules have been reviewed and the modifications of standard submodules to form the special submodules are scheduled to begin in October. The first special modules will be constructed in September but the only modification of these initial special modules is that they have special ITCs. Special modules with cut submodules will be fabricated starting in January.

Work also continued on the design of the support saddles and back cryostat support. A summary paper of the calculations has been written and detailed drawings of the support saddles have been fabricated. These will be discussed during an engineering meeting at CERN in September. The completed drawings and summary paper of the calculations can be found at the web page: http://gate.hep.anl.gov/vjg/.

1.4.1.3 Fixtures and Tooling
1.4.1.3.2 Production

David G. Underwood (Argonne National Lab.)

Some damage occurred to the electronics readout drawer at Argonne. This happened while the drawer was being moved between MSU modules at ANL and ANL modules for source testing for QC and optical repairs. Several components were scraped off the printed circuit board. The board was repaired at Argonne by the end of the month, but delays were incurred.

1.4.1.4 Testing

Milestone	Baseline	Previous	Forecast	Status
Beam test Series A	2-Oct-01	--	2-Oct-01	On Schedule
Modules Source Tested (40 Cum)	31-Dec-01	--	31-Dec-01	On Schedule

1.4.2 Extended Barrel Optics
1.4.2.1 Extended Barrel Scintillator
1.4.2.1.1 Design

Robert Miller (Michigan State University)

Optical Instrumentation Summary

Instrumentation of the US Tilecal extended barrel modules continued on an accelerated schedule in August. Two modules were completed at MSU and one was completed at ANL. A total of 37 modules have been instrumented, 36 have been tested, and 4 additional modules are in various stages of production.

Results of the certification scans continue to show rms tile-tile variations within readout cells of about 8%, comfortably better than the specified 10%.

1.4.2.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
100% Tile Deliveries from Russia Compl	2-Jul-01	--	2-Sep-01	Delayed (See #1)

Note #1 Tile production is completed in Russia. The sorting of tiles at CERN into lots for the 4 instrumentation sites has added a delay into the expected delivery schedule. This will not affect the module instrumentation schedule.

David G. Underwood (Argonne National Lab.)

Cs scans were completed on module ANL33 and module ANL 36 (the 17th one instrumented at ANL) was almost complete. An inventory of tiles was made to determine which tiles to use to minimize painting to match the light output. It was found that about 10% of the packs assigned to ANL were missing, and that we had about 10% packs which were assigned to either CERN or Barcelona. We continued inserting packs of batch 4A. There were additional delays due to damaged electronics drawer, bad tiles, and bad fibers. We are finding occasional tiles which have less light output at one end than at the other end. These tiles appear to have some damage on the edge where a mould mark is cut off.

Robert Miller (Michigan State University)

Tilecal module instrumentation at MSU proceeded at a faster rate in August due to the full time availability of the student workers. Modules ANL-35 and 37 were completed. Module 35 was scanned with the LED source. Module 31 and 35 were shipped to ANL in exchange for Modules 38 and 39. Both of the new modules were prepared for instrumentation, and had tiles and fibers inserted. Fibers were glued and polished in Module 37 and 38.

Planning was started at MSU for moving the Tilecal instrumentation to our new building in the spring of 2002. Shipping and handling of the modules will be much easier in the new lab facilities. Some delay in instrumentation is anticipated during the move, but this is not expected to significantly change the schedule for completion of the EB modules at MSU.

1.4.2.2 Extended Barrel Fibers

1.4.2.2.3 Production

David G. Underwood (Argonne National Lab.)

Fiber repairs were made on Module 33, and fibers were installed in module ANL-36. Several fibers were replaced due to damage in the area which is inside the aspirin tube. This occurred in spite of careful inspection of fibers before gluing. All the bad fibers came from one batch and one size, length B in the long profiles.

1.4.2.3 Optical Installation Fixtures

1.4.2.3.3 Production

David G. Underwood (Argonne National Lab.)

Some damage occurred to the electronics readout drawer at Argonne. This happened while the drawer was being moved between MSU modules at ANL and ANL modules for source testing for QC and optical repairs. Several components were scraped off the printed circuit board. The board was repaired at Argonne by the end of the month, but delays were incurred.

1.4.2.4 Supplies
1.4.2.4.3 Production — David G. Underwood (Argonne National Lab.)

An inventory of tiles of batch 4A was done. We found that we have enough tiles of some sizes for 6 more modules, and enough of other sizes for 8 more modules. Also, about 10% of the packs which were assigned to us are missing, and about 10% of the packs we have were originally assigned to either CERN or Barcelona. The main problem with these packs is that we cannot trust the light output data because we cannot trust the pack number on the pack. We do not want to install tiles which may not match adjacent tiles, and then have to remove them after the radioactive source measurements.

1.4.3 Readout
1.4.3.1 PMT Block
1.4.3.1.3 Production — Steven Errede (University Illinois-Urbana-Champaign)

We began STEP1 testing of Batch 6 PMTs ~ mid-August, 2001, after returning from Snowmass 2001. By the end of the month, we had tested 160 out of 250 PMTs from this batch, with 6 PMTs tentatively rejected thus far. We hope to complete the Step1 testing of this batch of Hamamatsu R7877 PMTs in early September.

1.4.3.2 Front-end 3-in-1 Card
1.4.3.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
3-In-1 Card Test 100% Complete	30-Nov-01	--	30-Nov-01	On Schedule

James Pilcher (University Of Chicago)

As reported previously, production of 3-in-1 cards by the vendor is complete and all cards have been received at Chicago for burn-in and testing.

In August 934 3-in-1 cards passed burn-in and testing and were shipped to CERN. This brings the overall number shipped to 7777 or 73% of the total. The monthly average over the 8-month period since burn-in and testing began is now up at 778 cards per month and our most recent 3-month running average is 966 per month. Our original estimates were for 867 per month. Thus our current throughput is above the expected rate and the long-term average should continue to climb slowly.

1.4.3.3 Front-end Motherboards
1.4.3.3.3 Production

Milestone	Baseline	Previous	Forecast	Status
MB Card Test 10% Complete	1-Mar-01	--	1-Oct-01	Delayed (See #1)
MB Card Fab 100% Complete	6-Apr-01	--	31-Aug-01	Completed
MB Card Test 25% Complete	1-May-01	1-Oct-01	1-Dec-01	Delayed (See #2)
MB Card Test 50% Complete	1-Aug-01	30-Nov-01	1-Feb-02	Delayed (See #3)
MB Card Test 100% Complete	24-Dec-01	24-Dec-01	1-Jun-02	Delayed (See #4)

Note #1-4 On track for current forecast and not on critical path.

James Pilcher (University Of Chicago)

In August we received the following numbers of Mother Board sections: 128 MB1, 119 MB2, 119 MB3, and 119 MB4. This brings the corresponding totals to: 271, 271, 271, 271, which is 100% of the order.

The final part of the Mother Board system is the small Mezzanine Card used for control purposes. The start of its production was delayed because of the delay in obtaining the CERN TTCrx ASIC. At this point the pre-production is complete and full production approved, all parts have been checked in at the assembly firm, the bare boards are being fabricated, and the surface mount work is complete. Volume deliveries should begin in early September. A total of 16 sets are on hand from the pre-production process.

A total of 15 sets of compete Mother Board systems have been burned in, tested and delivered to CERN. These have been used to equip the electronics drawers for the production calorimeter modules being calibrated in the test beam in August and September.

1.4.3.6 Read System Management

Milestone	Baseline	Previous	Forecast	Status
Test BM Calib of 4 Prod. Modls.	1-Oct-01	--	1-Oct-01	On Schedule

1.4.4 Intermediate Tile Calorimeter

1.4.4.1 Gap Submodules

1.4.4.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
Scintillator procurement	1-Oct-00	--	1-Oct-01	Delayed (See #1)
Start Scintillator Assembly	1-Dec-00	--	1-Nov-01	Delayed (See #2)
Ship submodules 37-40 to ANL	11-Jun-01	--	11-Aug-01	Completed (See #3)
Ship submodules 41-44 to ANL	27-Aug-01	27-Aug-01	27-Oct-01	Delayed (See #4)
Ship submodules 41-44 to BCN	3-Sep-01	--	3-Sep-01	On Schedule
Ship submodules 45-48 to ANL	26-Nov-01	--	26-Nov-01	On Schedule
Ship submodules 45-48 to BCN	17-Dec-01	--	17-Dec-01	On Schedule

Note #1 Prototypes of the ITC extension scintillators were tested at the CERN test beam last summer. Based on the test beam experience, we have made final modifications to the scintillator design. Procurement will follow as soon as final drawings are approved, and funding to buy extension scintillators are available at MSU.

Note #2 Prototypes of the ITC extension scintillators were tested at the CERN test beam last summer. Based on the test beam experience, we have made final modifications to the scintillator design. Assembly will follow as soon as funding to buy extension scintillators are available at MSU.

Note #3-4 Due to delayed startup of production in 1999, we are 2 months behind original schedule. There is no impact on module production.

Kaushik De (University Of Texas At Arlington)

We shipped 2 submodules each to Argonne and Barcelona, as scheduled. We also sent an extra submodule to Barcelona. We encountered a minor problem with one of the Argonne submodules. One of the bolts stripped on the weld bar while attaching the lifting fixture. The weld bar was repaired and new torque limits have been set to prevent any future occurrence.

We completed Step 1 testing of the second batch of PMTs. We are still waiting for hardware to run Step 2 (pulsed) tests.

Our technician, Victor Reece, spent two weeks at CERN to help with the installation of the light tight covers on the ITC side of completed modules. In the future, we expect to complete this step in the US before modules are shipped.

1.4.4.2 Cryostat Scintillators
1.4.4.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
Scintillator procurement	1-Dec-00	--	1-Dec-01	Delayed (See #1)
Start Scintillator Assembly	7-Sep-01	7-Sep-01	1-Nov-01	Delayed (See #2)
Management Contingency Go-Ahead	1-Oct-01	--	1-Oct-01	On Schedule

Note #1 Scintillator purchase and production of the ITC crack scintillators is delayed pending the decision to authorize this part of the project that was included in the management contingency fund. That decision is scheduled for 1 Oct. 2001. Funding for the mechanical components was approved in Feb. 2001, and those components will be purchase in FY 01.

Note #2 Purchase of the mechanical components for the crack scintillators is awaiting final checks by the ATLAS technical coordination team.

Robert Miller (Michigan State University)

Production of the ITC fiber assemblies continued during August. The final set of standard assemblies and the first 4 sets of assemblies for special modules were shipped to Barcelona.

Final drawings of the crack scintillator mechanical components were made and requests for quotes were sent to potential sources. A final check of the dimensions and mounting positions for these scintillators was requested of the ATLAS technical coordination team. The purchase orders for these components will be issued as soon as we get the go ahead from the TC.

1.5 MUON

Milestones with changed forecast dates:

1.5.7.2.1 Faraday Cages

Milestone	Baseline	Previous	Forecast	Status
Finished Faraday Cage Designs	21-Dec-00	22-Aug-01	22-Nov-01	Delayed (See #1)

Note #1 FC for EIL1 is complete and parts have been made. Designs of FC for the 3x8x8.5, 3x8x14 and 4x6x 8.5 Deg chambers have been completed and released for production for the FC bases. Final design of HV feed-in box is underway. Quotes for the remaining production parts are being evaluated.

1.5.7.2.2 Gas System

Milestone	Baseline	Previous	Forecast	Status
Finish Gas System Design	7-Jun-01	15-Aug-01	28-Sep-01	Delayed (See #1)

Note #1 Design efforts now focus on design of the gas system for the special chambers with cutouts. Design of the gas tube routing between the gas block and the gas manifold is underway.

1.5.7.2.4 Chamber Analysis

Milestone	Baseline	Previous	Forecast	Status
Finish FEA Modeling	30-Aug-01	30-Aug-01	30-Nov-01	Delayed (See #1)

Note #1 This work has been delayed because the final wheel structural designs are not yet available.

1.5.7.2.5 design of Special Chamber Tooling

Milestone	Baseline	Previous	Forecast	Status
Finish all Special Chamber Tooling	27-Sep-01	27-Sep-01	28-Dec-01	Delayed (See #1)

Note #1 Completion of this task will probably be delayed but will be ahead of need. Work is concentrated at Brandeis on EMS3 - the first special chamber that will be constructed.

1.5.8.1.3 Integ with Support Structure

Milestone	Baseline	Previous	Forecast	Status
50% Complete	1-Aug-01	1-Aug-01	1-Nov-01	Delayed (See #1)

Note #1 Delayed for same reasons as noted above.

1.5.9.2.1 Signal Hedgehog 3X8

Milestone	Baseline	Previous	Forecast	Status
Hedgehog PCB Certified	30-Aug-00	1-Aug-01	1-Oct-01	Delayed (See #1)

Note #1 Delayed to implement design changes: shortening, coating change, and capacitor vendor switch (Tucsonix to Murata).

1.5.9.4 Chamber Service Module

Milestone	Baseline	Previous	Forecast	Status
CSM-1/Octal ASD/MROD Test	1-Dec-01	1-Dec-01	1-Jul-02	Delayed (See #1)

Note #1 Testing will follow CSM-1 prototype completion and will use already tested production mezz boards with AMT-2 and the octal ASD.

1.5.12.2.3 H8 DATCHA

Milestone	Baseline	Previous	Forecast	Status
H8 Operational	24-Nov-00	1-Sep-01	15-Nov-01	Delayed (See #1)

Note #1 The assembly of support structures and frames at CERN has been slower than expected. This is now completed but the area will be unavailable for mounting devices for much of October because the beam will be on. Most components are expected to arrive in October.

1.5.12.4.5 EIS1 (Boston)

Milestone	Baseline	Previous	Forecast	Status
Ship to Site	16-Feb-01	1-Sep-01	31-Aug-01	Completed

1.5.12.4.17 EMS2 (Seattle)

Milestone	Baseline	Previous	Forecast	Status
Ship to Site	23-Jan-01	1-Sep-01	31-Aug-01	Completed

1.5.4 CSC Chambers

1.5.4.4 CSC Construction

Milestone	Baseline	Previous	Forecast	Status
Start CSC Chamber Production	1-Mar-01	--	1-Sep-01	Delayed (See #1)

Note #1 Start of production will likely slip further pending completion of the work on documentation, procurement specification, and other open issues identified during the November 27 PRR.

Venetios Polychronakos (BNL)

We have received all parts for the first 4 production chambers and construction is starting in early September on schedule. The first four chambers are expected to be completed on schedule by the end of the calendar year. The allowed time is three to four times longer than the estimated time needed at production speed. The reason is our plan to measure in detail far more parameters in order to confirm that the manufacturers have met specifications and our assembly procedures fully debugged.

The procurement process for the bulk of the chambers is well advanced and we expect to award the contracts in the next couple of months with an expected delivery starting early next year. Finshing half of the base chambers on schedule by the middle of 2002.

We have one spare precision cathode which we do not plan to use. Its dimensional stability will be checked on a coordinate measurement machine every couple of months to determine any long term effects.

1.5.4.4.1 CSC1

Milestone	Baseline	Previous	Forecast	Status
4 Chambers Complete	1-May-01	--	1-Dec-01	Delayed (See #1)
16 Chambers Complete	2-Oct-01	--	30-Apr-02	Delayed (See #2)

Note #1-2 This milestone follows the delay in start of construction, now scheduled for September 1.

1.5.4.5 CSC Support Structure

Milestone	Baseline	Previous	Forecast	Status
Start Support Structures Construction	3-Jan-01	--	3-Dec-01	Delayed (See #1)

Note #1 The small wheel fabrication is expected to be launched by the end of the year. The contract and follow-up will be CERN responsibility.

Venetios Polychronakos (BNL)

We are in the process of finalizing the services routing working with the CERN group in charge of the support structure production. In parallel the FEA calculations for a final check after the latest design change are proceeding.

1.5.7 MDT Chamber Production

1.5.7.1 Enginering Management

1.5.7.1.1 Chamber Integration Drawings

Milestone	Baseline	Previous	Forecast	Status
Complete Chamber Integration Drawings	1-Jul-01	--	1-Oct-01	Delayed (See #1)
Chamber Integration Drawings	28-Sep-01	--	28-Sep-01	On Schedule
Chamber Integration Drawings	28-Sep-01	--	28-Sep-01	On Schedule

Note #1 The rate of creating chamber integration drawings has been delayed due to loss of a designer in the BMC engineering office.

Richard Coco (MIT)

The mechanical design effort continues to create the chamber assembly drawings for EMS4 and EMS2. The assembly drawing for chamber EIS1 Side A was completed during this reporting period.

The effort has been slowed by the loss of a designer in the engineering office due to budgetary constraints.

1.5.7.1.2 Engineering Documentation — Richard Coco (MIT)

Engineering documentation efforts are focused on creating top-level chamber assembly drawings for the Series 2 EIS1, EMS4 and EMS2 chambers. During this reporting period the Side A EIS1 assembly drawing was completed. Work is progressing on the EMS4 and EMS2 chamber drawings.

Activities are also in process to complete the FC design for the various chambers. The pre-production FC parts for the EIS1 chamber were received and fitted successfully of the first chamber of this series constructed at BMC.

FC mezz card boxes, HV inlet box, gas manifold cover panel and RO side HHC FC covers are the remaining open design for the FC.

Design of the FC base plates required for installing the chamber gas system have been completed, verified by fitting pre-production parts on the appropriate chambers and released for production.

1.5.7.1.4 QA/QC Engineering Support — Richard Coco (MIT)

Engineering QA/QC support is provided to the MDT chamber assembly sites as requested.

1.5.7.1.5 Project Engineering — Richard Coco (MIT)

The MDT chamber engineering group will lose a full time designer effective at the end of this FY due to budget constraints. This will require prioritizing of design tasks in order to most efficiently use the remaining designer assigned to the project at BMC.

Project engineering has been actively working to develop schedules, manpower needs and cost estimates for the M&O phase of the MDT program at CERN

1.5.7.2 Design of Chambers and Tooling

1.5.7.2.1 Faraday Cages

Milestone	Baseline	Previous	Forecast	Status
Finished Faraday Cage Designs	21-Dec-00	22-Aug-01	22-Nov-01	Delayed (See #1)
Faraday Cage	28-Sep-01	[New]	28-Sep-01	On Schedule

Note #1 FC for EIL1 is complete and parts have been made. Designs of FC for the 3x8x8.5, 3x8x14 and 4x6x 8.5 Deg chambers have been completed and released for production for the FC bases. Final design of HV feed-in box is underway. Quotes for the remaining production parts are being evaluated.

Richard Coco (MIT)

Design of the major components of the FC has been completed and parts are in production.

Remaining design efforts are required for the FC shielding surrounding the HV supply. Mezz card boxes and the cover which encloses the gas manifold bar. These efforts await final design inputs for the electronics.

1.5.7.2.2 Gas System

Milestone	Baseline	Previous	Forecast	Status
Finish Gas System Design	7-Jun-01	15-Aug-01	28-Sep-01	Delayed (See #1)
Gas System	15-Aug-01	[New]	28-Sep-01	Delayed (See #2)
Gas System	28-Sep-01	[New]	28-Sep-01	Delayed (See #3)

Note #1 Design efforts now focus on design of the gas system for the special chambers with cutouts. Design of the gas tube routing between the gas block and the gas manifold is underway.

Note #2 The remaining gas system components to be designed are the gas feed lines located on the chambers. This effort should be completed by the end of this FY.

Note #3 Completion of the gas system design has been delayed and is now scheduled to be competed by the end of the FY.

Richard Coco (MIT)

The design of all major gas system components has been completed except for the 6 mm OD, 4 mm ID gas distribution line required to carry gas from the chamber gas inlet block to each multilayer gas manifold.

This design effort should be completed during the next reporting period.

1.5.7.2.3 Spacer Frame Design

Milestone	Baseline	Previous	Forecast	Status
Finish Spacer Frame Design	17-Jan-02	--	17-Jan-02	On Schedule

1.5.7.2.4 Chamber Analysis

Milestone	Baseline	Previous	Forecast	Status

Finish FEA Modeling	30-Aug-01	30-Aug-01	30-Nov-01	Delayed (See #1)

Note #1 This work has been delayed because the final wheel structural designs are not yet available.

1.5.7.2.5 Design of Special Chamber Tooling

Milestone	Baseline	Previous	Forecast	Status
Finish all Special Chamber Tooling	27-Sep-01	27-Sep-01	28-Dec-01	Delayed (See #1)

Note #1 Completion of this task will probably be delayed but will be ahead of need. Work is concentrated at Brandeis on EMS3 - the first special chamber that will be constructed.

1.5.7.3 Tooling

1.5.7.3.1 Module 0-Precision Tooling

1.5.7.3.3 Series Production Precision Tooling

Milestone	Baseline	Previous	Forecast	Status
Finish Series Production Tooling	1-Feb-01	--	15-Jan-02	Delayed (See #1)

Note #1 Design work for the series 3 production is underway. The tooling design remains off the critical path.

1.5.7.3.5 BMC Tube Assembly Station — Frank Taylor (MIT)

The BMC tube assembly station continues to work smoothly.

1.5.7.3.8 BMC Tube Test Station — Frank Taylor (MIT)

Improvements in the gas distribution system have been designed by Brandeis and MIT and are under construction at Harvard. The pocan plastic 1/2 jumpers will be replaced by a pocan gas block. This arrangement should be more robust.

A dry box around the dark current measuring device is under consideration to improve the dark current measurements during very humid conditions. During these times many spurious dark current failures have been observed and the through-put of the dark current QA process impeded.

1.5.7.3.11 BMC Chamber Assembly Station — Krzysztof Sliwa (Tufts University)

Machining of a new set of sphere blocks and ancillary jigging was started at the beginning of the month.

Tufts continues to machine assorted components for the alignment system in coordination with Hermann Wellenstein of Brandeis. During third week of the month, a request for machining of one set of four spacer frame-setting blocks was received from the University of Washington group. Tufts took on the machining of these pieces, which were completed and shipped by August 25, 2001.

1.5.7.3.13 Seattle Chamber Assembly Station — Henry Lubatti (University of Washington)

We completed 1211 EMS2A 14 tubes in August.

1.5.7.4 Prototype Chamber Fabrication

1.5.7.4.1 Mod-0 EIL (BMC) — Alex Marin (Boston University)

Steve Ahlen wrote a detailed report on the Cosmic Ray Stand experience. Please look on http://www.hepl.harvard.edu/~atlas_chamber/.

1.5.7.6 Common Procurement

1.5.7.6.1 Procurement of Tubes — Tom Fries (Harvard University)

The first 3 series of tubes have been received at each of the US assembly sites.

1.5.7.6.2 Procurement of Wire — Tom Fries (Harvard University)

No additional wire was received during August.

1.5.7.6.3 Procurement of Endplugs — Tom Fries (Harvard University)

9,200 NIEF endplugs were received and distributed among the U.S. sites.

Meanwhile 10,924 MPI-type endplugs delivered in July, were determined to be acceptable and will be distributed among the US sites providing a 6-week buffer inventory.

Frank Taylor (MIT)

The MPI backup endplugs were tested at the BMC stringer station by making 24 tubes and running them through the complete QA process. Only one tube failed because a twister was not installed in one of the endplugs (operator error). On the basis of this test the MPI endplugs were declared to be useable as emergency spares. Approximately 3,700 endplugs will be distributed to each of the U.S. tube production sites.

1.5.7.6.4 Procurement of Faraday Cage — Tom Fries (Harvard University)

EIS1/2 - prototypes were approved and some of the production pieces (16 chamber's-worth) were received by EOM at BMC. The balance is expected to ship by mid-September.

EML2 - production pieces (16 chamber's-worth) were received at UW.

EMS2, EMS4 & EMS5 - some of the production pieces (48 chamber's-worth) were received by EOM at UM & UW. The balance is expected to ship by mid-September.

Note: Complete sets of FCs are not yet through design. Details are yet to be worked out for the Read-Out Covers, Gas Panels and High-Voltage Entrance parts (3).

1.5.7.6.5 Procurement of Gas Supply System — Tom Fries (Harvard University)

Tubelets:

The European supplier (Heim) has delivered 13% of their order. This order accounts for roughly 70% of our total tubelete requirement.

Gas Bars (from UW machine shop):

28 EMS-5 Type 2 were shipped to UM.

1.5.7.7 BMC Chamber Construction 104

1.5.7.7.1 EIL 1 Series (WBS 1.5.7.7.1)

Milestone	Baseline	Previous	Forecast	Status
End of EIL1 series production	14-Jun-01	--	14-Jun-01	Completed (See #1)

Note #1 EIL1 bare chambers completed. No parts for services available at this time. Brandeis mounted the gas type III components on EIS1.01, reaching the ATLAS leak requirement.

1.5.7.7.2 EIS1 Series (WBS 1.5.7.7.2) — Frank Taylor (MIT)

Approximately 2368 tubes have passed QA for EIS1 BMC chamber production. This corresponds to module 7. Tube production continues to be routine. A spare spark gap has been delivered. Some improvements in the gas distribution system of the dark current device have been designed by the Brandeis and MIT teams and is under construction at Harvard. A spare filament for the Brandeis Schublade batch leak tester is on order. One of two pairs is burnt out. A third technician will be hired this fall.

Alex Marin (Boston University)

As of August 31, three EIS1 base chambers were assembled. No services were installed.

1.5.7.8 WBS 1.5.7.8 Michigan Chamber Construction 104

1.5.7.8.2 EMS4 Series (WBS 1.5.7.8.2) — Ed Diehl (University of Michigan)

During August we continued EMS4 production. Production continued smoothly and by month's end a total of 5 EMS4 chamber had been glued. We had hoped to begin installing Faraday cages and gas bars by month's end but could not due to a delay in Faraday cage production. When Faraday cages become available we will install them (and gasbars) on all EMS4 chambers. We may halt chamber gluing for one week in order to concentrate on the FC installation. We are reaching the limit of how many chambers we can store locally. We hope the FC and gas systems can be installed and tested fairly quickly, in which case we'll ship a container with 6 chambers to CERN in October.

1.5.7.9 WBS 1.5.7.9 Seattle Chamber Construction 96

1.5.7.9.3 EMS2 Series (WBS 1.5.7.9.3) — Paul Mockett (University of Washington)

Seattle August Chamber Production 1.5.7.9.3

Finished construction of EMS2.A04, Chamber 2, except for gas and electronic services.

Finished construction of EMS2.A06, Chamber 3, except for gas and electronic services.

Finished construction of EMS2.A08, Chamber 4, except for gas and electronic services.

Finished construction of EMS2.A10, Chamber 5, through ML2, layer 2 base gluing.

Installed Optics on various EMS2 spacer frames along with calibration and verification of their operation.

Repair of misplaced Peemo camera gun mounts on EMS2.A10 chamber. We machined off a portion of a replacement base and glued it next to the base incorrectly mounted

Completed installation and plumbing, except for gas blocks and leak checking, on 6 EML2 chambers. This includes installation of base faraday cages, gasbars and tubelets as well as removal of old bases, gas bars and tubelets on some of these chambers.

Created drawing for tubelet half jumper assembly fixture and submitted into shop for construction. Fixture is about 75% complete.

Performed the usual efforts on repair and upgrades to assembly electronics and software.

Began effort to read out chamber elx with CSM. So far unsuccessfully.

Henry Lubatti (University of Washington)

We completed 1211 EMS2A 14 tubes in August.

1.5.8 MDT Supports

1.5.8.1 Mechanical Design

1.5.8.1.3 Integ with Support Structure

Milestone	Baseline	Previous	Forecast	Status
(SM Wheel) CERN Design/FEA Complete	15-Jul-00	--	1-Dec-01	Delayed (See #1)
(Big Wheel) CERN Design/FEA Complete	1-Feb-01	--	15-Dec-01	Delayed (See #2)
50% Complete	1-Aug-01	1-Aug-01	1-Nov-01	Delayed (See #3)

Note #1 A large fraction of this work has been completed, but as we depend on CERN for the detailed small wheel design from CERN and others for alignment bar and plumbing information we have a delay. Some small progress was made in July. We forecast that this will not be completed until December 1, 2001. (Situation unchanged since July 01 report.)

Note #2 Because we depend on CERN for the detailed big wheel design and others for alignment bar and plumbing information we have a delay. We forecast that this will not be completed until March 15,2002. The May design report on the Big Wheel showed much progress but the final drawings and bid

specs will not likely be available until Dec, 15, 2001. It is expected that there will be further design and installation changes during the bid process. (Status unchanged since July 01 report.)

Note #3 Delayed for same reasons as noted above.

1.5.9 MDT Electronics

1.5.9.1 Mezzanine Card

1.5.9.1.1 MDT-ASD

Milestone	Baseline	Previous	Forecast	Status
ASD PRR	19-Oct-01	--	19-Oct-01	On Schedule

George Brandenburg (Harvard University)

6 ASD01a prototype chips have been successfully tested. All seems to be OK, except the adjustable deadtime which is shorter than expected (approx equal to the total drift time). It is under discussion whether this presents any problems.

1.5.9.1.2 Mezz PCB

Milestone	Baseline	Previous	Forecast	Status
Mezz PCB Certified	16-Nov-01	--	16-Nov-01	On Schedule

George Brandenburg (Harvard University)

The current plan is to have only three mezz board types for final production: one 3x8 design which works both for type I and II hedgehogs, and two 4x6 designs which work for type III and IV hedgehogs respectively. The mezz-csm cable connector would in all three cases be oriented parallel to the plane of the chamber. This way the cable can lay flat on the top surface of the FC and exit at a right angle to the spacer frame area. The prototype layouts for types II and IV have been completed and submitted for board fabrication. Before submission an adjustment was made to the width of the boards reducing this from 124mm to 113mm (at the request of the Rome group, which needed the space for cable routing).

1.5.9.2 Hedgehog Cards

1.5.9.2.1 Signal Hedgehog 3X8

Milestone	Baseline	Previous	Forecast	Status
Hedgehog PCB Certified	30-Aug-00	1-Aug-01	1-Oct-01	Delayed (See #1)
Hedgehog Production Complete	28-Feb-01	--	31-Dec-02	Delayed (See #2)

Note #1 Delayed to implement design changes: shortening, coating change, and capacitor vendor switch (Tucsonix to Murata).

Note #2 Production will most likely now take place at CERN starting in the last quarter of 2001. The first production quantities should be available at the end of 2001. Production will continue during 2002 in parallel with chamber building.

1.5.9.3 Patch Panels

1.5.9.3.1 Signal Patch Panel — George Brandenburg (Harvard University)

Patch panels are no longer planned. This item covers the csm-mezz cables, which will be made with shielded, halogen-free ribbon cable. Cable samples have been received and will be tested with octal mezz prototypes.

1.5.9.4 Chamber Service Module

Milestone	Baseline	Previous	Forecast	Status
CSM-1 Prototype	1-Sep-00	--	1-Jun-02	Delayed (See #1)
CSM-1/Octal ASD/MROD Test	1-Dec-01	1-Dec-01	1-Jul-02	Delayed (See #2)

Note #1 The scope of the CSM-1 has recently changes to a simpler, more robust design. As a result the completion date of the first prototype has moved to spring 02. Work on the design for this more ambitious design is progressing.

Note #2 Testing will follow CSM-1 prototype completion and will use already tested production mezz boards with AMT-2 and the octal ASD.

1.5.11 CSC Electronics

1.5.11.1 ASM1 Boards

1.5.11.1.1 Design

Milestone	Baseline	Previous	Forecast	Status
Preamp/Shaper Final Design Review	2-Oct-01	--	1-Dec-01	Delayed (See #1)
System Critical Design Review	2-Oct-01	--	1-Dec-01	Delayed (See #2)

Note #1-2 Delayed to allow us to verify design modifications to preamp/shaper for yield enhancement, reduced crosstalk, and improved overload recovery.

Anand Kandasamy (BNL)

Redesign of ASM I and accompanying FLEX cable for ASM I to ASM II are being in the process of redesign for the new 25 channel Preamp/Shaper ASIC.

CSC Chamber calibration and certain auxiliary monitoring systems are being designed and in the process of fabrication and testing.

Test Bench systems are being designed for testing of ASM PACKS.

- High current power supplies (only for testing ASM Packs)

- Charge Injection boards for pulsing 192 channels simultaneously.

- Current monitoring circuitry

- Faraday Cage and Cooling, mechanical constraints

1.5.11.2 ASM II Board

1.5.11.2.1 ASM II Board Design — Anand Kandasamy (BNL)

ASM II B (192 channel prototype) PCB is being drafted by the CAD group. VME DAQ board is being debugged and tested to acquire data stream from the optics and store it in a disk.

1.5.11.4 Sparsifiers

1.5.11.4.2 Sparsifier Prototype

Milestone	Baseline	Previous	Forecast	Status
Sparsifier 1st Proto in Hand	1-Aug-01	--	15-Aug-01	Completed

1.5.11.5 ROD's

1.5.11.5.1 ROD Design — David Stoker (University of California Irvine)

During August, we continued coding of the SPU (Sparsifier Processing Unit) C and assembly code. We continued C coding of the Clock Generation drivers, which run in the ROD's HPU (Host Processing Unit). In addition, began C coding of the FPGA Configuration driver, which runs in the HPU and is used to configure all of the FPGAs on the ROD. The prototype ROD motherboard printed circuit boards were received, and we began incremental assembly and testing of the ROD motherboard. We also worked on preparation for the ROD software Conceptual Design Review.

1.5.11.5.2 ROD Prototype

Milestone	Baseline	Previous	Forecast	Status
RODs 1st Proto in Hand	2-Apr-01	--	15-Aug-01	Completed

1.5.11.7 Software

1.5.11.7.1 Software Design

Milestone	Baseline	Previous	Forecast	Status
S/W Conceptual Design Review	2-May-01	--	1-Oct-01	Delayed (See #1)

Note #1 Development of code external to ROD and documentation not ready for review.

1.5.12 Global Alignment System — Jim Bensinger (Brandeis University)

Substantial progress was made on H8 and the development of the new (Long Wire - V2) alignment DA system. Two phantom chambers were mounted in H8 and internal monitors are being read out successfully. The first 9.6-meter alignment bar arrived at CERN. Several new header boards were produced and tested.

The complete set of inplane and proximity mounts for all of the second round of chamber production have now been shipped to the sites.

1.5.12.1 Global Design

1.5.12.1.1 Alignment Bars

Milestone	Baseline	Previous	Forecast	Status
Alignment Bar Design Complete	30-Mar-01	--	30-Mar-02	Delayed (See #1)

Note #1 Design for H8 is complete and there is no work on this item at this time. This design will be reviewed following analysis of H8 results. (By then we hope TC will stop moving the wheels around.) Final design will take place at that time.

Jim Bensinger (Brandeis University)

The measurement of the first complete alignment bar (all internal sensors and external sensor mounts) were completed at Freiburg and shipped to CERN. Detailing of the other bars is continuing at Brandeis and measurements are continuing at Freiburg.

Design of the EI bars is continuing. This is complicated by the distance from the bar to the alignment line, much larger than in the other layers.

1.5.12.1.2 Proximity Monitors

Milestone	Baseline	Previous	Forecast	Status
Proximity Monitor Design Complete	29-Sep-00	--	7-Aug-01	Completed

Jim Bensinger (Brandeis University)

The design of the proximity (H8 version) was completed and submitted to the shop. Completed cameras are expected next month.

1.5.12.1.3 Multi-Point System (BCAM)

Milestone	Baseline	Previous	Forecast	Status
BCAM Design Complete	31-Dec-01	--	31-Dec-01	On Schedule

Jim Bensinger (Brandeis University)

The first set of BCAMs bodies was received from the machine shop. The laser driver (BCAM Peripheral Head) boards were completed and tested. The BCAM head is expected next month.

1.5.12.1.4 System Design **Jim Bensinger (Brandeis University)**

Several issues were addressed: (1) completion of the H8 layout, (2) response to moves of the big and small wheels by technical coordination, (3) preparation of an engineering change request for changes to the struts and voussoirs, (4) meetings with muon integration team to review assembly and construction of the small and big wheels.

1.5.12.1.5 DAQ

Milestone	Baseline	Previous	Forecast	Status
Complete design of H8 alignment DAQ hardware.	1-Apr-01	--	1-Aug-01	Completed
DAQ Design Complete	28-Sep-01	--	30-Mar-02	Delayed (See #1)

Note #1 The H8 version basic design is complete. This design will be re-evaluated following analysis of H8 data and, if needed, will be revised at that time.

Jim Bensinger (Brandeis University)

Work continues on the Long Wire Alignment DAQ. Several new circuits were produced; the BCAM peripheral head, and the device multiplexer. The production version of the inplane sensor header was produced.

1.5.12.2 Operational Test Stands

1.5.12.2.3 H8 DATCHA

Milestone	Baseline	Previous	Forecast	Status
H8 Operational	24-Nov-00	1-Sep-01	15-Nov-01	Delayed (See #1)

Note #1 The assembly of support structures and frames at CERN has been slower than expected. This is now completed but the area will be unavailable for mounting devices for much of October because the beam will be on. Most components are expected to arrive in October.

Jim Bensinger (Brandeis University)

Work continued on H8. The 6th phantom chamber was sent to CERN. Two chambers were mounted on the EO structure. Lessons learned were applied to the plans for chamber installation. The LW-DAQ system was setup at H8, several problems were observed and overcome. Long term monitoring of the alignment devices has begun.

1.5.12.3 Global System Production

Milestone	Baseline	Previous	Forecast	Status
Align Bar/Prox Monitors PRR	3-Jan-01	--	31-Mar-02	Delayed (See #1)
Critical System Design Review	3-Jan-01	--	31-Mar-02	Delayed (See #2)

Note #1-2 Not yet scheduled but will follow analysis of H8 results.

Jim Bensinger (Brandeis University)

The part of system production that has begun is that relating to the production of MDT chambers, the inplane system and the camera mounts and mask mounts for the proximity monitors that go on the chambers.

1.5.12.3.1 Alignment Bars

Milestone	Baseline	Previous	Forecast	Status
Bar Production 10% Complete	1-Oct-01	--	1-Jun-02	Delayed (See #1)

Note #1 This is no longer a U.S. responsibility and will be done at Freiburg. Bar production will not begin until after analysis of H8 results.

1.5.12.3.2 Proximity Monitors

Milestone	Baseline	Previous	Forecast	Status
Prox. Production 10% Complete	1-Jan-02	--	1-Jan-02	On Schedule

Jim Bensinger (Brandeis University)

We have delivered all the mask and camera mounts for the second round of production to the US production sites.

1.5.12.3.3 Multi-Point System (BCAM)

Milestone	Baseline	Previous	Forecast	Status
BCAM Production Begins	1-Jan-02	--	1-Jan-02	On Schedule

1.5.12.3.4 DAQ

Jim Bensinger (Brandeis University)

This month we fabricated prototype amounts of the following PCBs:

A2034 Inplane Mask Head

A2031 Device Driver

A2040 BCAM Peripheral Head

A2033 Proximity Sensor Head

A2030 Device Multiplexer

A2041 LED Array

And produced productions amounts of the A2036 Inplane Sensor Head

1.5.12.4 MDT Inplane Monitors

1.5.12.4.1 Common Items

Milestone	Baseline	Previous	Forecast	Status
Common Items 25% Complete	1-Jan-02	--	1-Jan-02	On Schedule

Jim Bensinger (Brandeis University)

Almost all of the common parts for the approved MDT chamber production now exist at Brandeis or on produced chambers.

1.5.12.4.5 EIS1 (Boston)

Milestone	Baseline	Previous	Forecast	Status
Ship to Site	16-Feb-01	1-Sep-01	31-Aug-01	Completed

Jim Bensinger (Brandeis University)

All inplane kits for this chamber have been delivered to Harvard.

1.5.12.4.6 EIS2 (Boston)

Milestone	Baseline	Previous	Forecast	Status
Ship to Site	23-Oct-01	--	1-Feb-02	Delayed (See #1)

Note #1 Changes in MDT production schedule has moved this chamber to the third round of production. Since this is a special chamber, confirmation of the inplane design will await completion of the design of the chamber.

1.5.12.4.13 ENL3 (Michigan)

Milestone	Baseline	Previous	Forecast	Status
Ship to Site	10-Dec-01	--	10-Dec-01	On Schedule

1.5.12.4.17 EMS2 (Seattle)

Milestone	Baseline	Previous	Forecast	Status
Ship to Site	23-Jan-01	1-Sep-01	31-Aug-01	Completed

Jim Bensinger (Brandeis University)

All inplane kits for this chamber have been delivered to Seattle.

1.5.12.4.18 EMS3 (Seattle)

Milestone	Baseline	Previous	Forecast	Status
Ship to Site	7-Sep-01	--	1-Apr-02	Delayed (See #1)

Note #1 This chamber is not scheduled to be built until the third round of MDT production.

1.5.12.4.19 EMS4 (Michigan)

Jim Bensinger (Brandeis University)

All inplane kits for this chamber have been delivered to Michigan. Two central lens gave out of focus images and have been returned to Brandeis to be investigated.

1.6 TRIGGER

Milestones with changed forecast dates:

Milestone	Baseline	Previous	Forecast	Status
LVL2 Trigger Design Complete	31-Dec-01	31-Dec-01	31-Dec-02	Delayed (See #1)
Start Production	8-Jan-02	8-Jan-02	8-Jan-03	Delayed (See #2)

Note #1 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. The TDR is scheduled for the end of Dec. '02. This is the earliest date possible for a complete design.

Note #2 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. The production will start after design is complete.

1.6.1.2.4 SRB Prototype Travel

Milestone	Baseline	Previous	Forecast	Status
Prototype SRB Assy Compl	30-Sep-01	30-Nov-01	31-Oct-01	Delayed (See #1)

Note #1 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype integration is now expected to be completed at the end of October

1.6.3.2 SCT Protos

Milestone	Baseline	Previous	Forecast	Status
Prototype SCT Assy Compl	30-Sep-01	30-Sep-01	31-Oct-01	Delayed (See #1)

Note #1 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype integration is now expected to be completed at the end of October.

Milestone	Baseline	Previous	Forecast	Status
LVL2 Trigger Prototype Complete	30-Sep-01	--	31-Oct-01	Delayed (See #1)
LVL2 Trigger Design Complete	31-Dec-01	31-Dec-01	31-Dec-02	Delayed (See #2)
Start Production	8-Jan-02	8-Jan-02	8-Jan-03	Delayed (See #3)

Note #1 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype integration is now expected to be completed at the end of October

Note #2 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. The TDR is scheduled for the end of Dec. '02. This is the earliest date possible for a complete design.

Note #3 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. The production will start after design is complete.

1.6.1 LVL2 SRB

1.6.1.2 SRB Protos

1.6.1.2.1 SRB Protos EDIA **Robert Blair (Argonne National Lab.)**

The design of a Gigabit ethernet based link card for use with level 1 interface tests is proceeding. Use of Gigabit ethernet is considered optimal since its use within the supervisor allows for commodity hardware to be used in supervisor processors. The card under design will include a significant amount of buffering and will be FPGA based and reasonably flexible. This will allow for it to act as a prototype for use in the ROS as well as allowing it to be used within the Supervisor. The plan is to integrate Gigabit ethernet receivers and drivers on the RoI Builder. This will keep costs down and allow for a uniform technology choice for the physical links.

Bernard Pope (Michigan State University)

The ROD working group activity was concentrated on the definition of the ROD crate controller functionality and the recommendation of a standard ROD crate controller. The ROD working group web page was updated including a ROD working group mailing list and a "Task Force" summary page.

1.6.1.2.4 SRB Prototype Travel

Milestone	Baseline	Previous	Forecast	Status
Prototype SRB Assy Compl	30-Sep-01	30-Nov-01	31-Oct-01	Delayed (See #1)

Note #1 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype integration is now expected to be completed at the end of October

1.6.2 LVL2 Calorimeter Trg

1.6.2.1 Calo Design

1.6.2.1.1 Calo Design EDIA — Saul Gonzalez (University Of Wisconsin)

During August, the StoreGate interface to the Transient Event Store as implemented in the calorimeter trigger prototype code.

1.6.2.2 Calo Protos

Milestone	Baseline	Previous	Forecast	Status
Prototype Calo Assy Compl	30-Sep-01	--	31-Oct-01	Delayed (See #1)

Note #1 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype integration is now expected to be completed at the end of October

1.6.3 LVL2 SCT Trg

1.6.3.1 SCT Design

1.6.3.1.1 SCT Design EDIA — Brigitt Schmid (University Of Calif. At Irvine)

Study of alternative implementations of the ROD/ROB interface continued in August. Investigations of the user requirements of the various ATLAS ROD developments regarding Readout Link specifications (bandwidth, protocol, physical implementation of interface) continued in the context of the ATLAS ROD Working Group Readout Link Task Force. All ROD developments surveyed to date can accommodate an interface via a connector to a mezzanine card or transition module. An interface via a connector with electrical and protocol specifications is preferred by the task force for reasons of flexibility and upgradability. Small updates were made to our earlier conceptual design of a ROBin that can be mounted on RODs in order to eliminate the need for Readout Links. A variation of this design that would provide

sufficient bandwidth for event building at the full LVL1 trigger rate was developed. Study of the system implications of a network-based Readout Subsystem (ROS) with the ROS working group continued.

1.6.3.1.4 SCT Design Travel

Milestone	Baseline	Previous	Forecast	Status
SCT for Integ Study Compl	30-Sep-01	--	30-Nov-01	Delayed (See #1)

Note #1 This prototype preliminary exploitation has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype evaluation is now expected to be completed at the end of November.

1.6.3.2 SCT Protos

Milestone	Baseline	Previous	Forecast	Status
Prototype SCT Assy Compl	30-Sep-01	30-Sep-01	31-Oct-01	Delayed (See #1)

Note #1 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype integration is now expected to be completed at the end of October.

1.6.4 Architecture & LVL2 Global Trigger

1.6.4.1 Arch. Design

1.6.4.1.1 Arch. Design EDIA — Brigitt Schmid (University Of Calif. At Irvine)

Work continued with TDAQ system leaders on project planning for the development and prototyping period preceding the HLT/DAQ/DCS TDR. Preliminary work breakdown structures were developed for the Data Collection and HLT Dataflow subsystems. Planning and preparation for the TDAQ Activity/System Status Overview (ASSO) that will be held in October started.

In order to understand the range of possible solutions for the dataflow network, we met with Cisco Systems to discuss possible network topologies, present and future Cisco switches, and possible collaboration. We also looked at topologies that would incorporate network-based Readout Subsystems.

Bernard Pope (Michigan State University)

Work continued on the message passing implementation: a first version of a TCP implementation was finished. Code to initialize the message passing from the configuration database was added. The configuration database interface was changed to be compatible with the Online Software conventions.

Administrative work included the beginning of a WBS structure for Data Collection based on the original task list which ATLAS management requires for the October Atlas System Status Overview (ASSO) of TDAQ.

1.6.4.1.4 Arch. Design Travel

Milestone	Baseline	Previous	Forecast	Status
Prototype Project Assy Compl	30-Sep-01	--	31-Oct-01	Delayed (See #1)

Note #1 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype integration is now expected to be completed at the end of October

1.6.4.2 Global Production

1.6.4.2.1 Global Prod Eqmt — Saul Gonzalez (University Of Wisconsin)

After finishing the instrumentation of the Athena framework, W. Wiedenmann proceeded to instrument the byte-stream converters needed for the Event Filter and provided by the Barcelona group. This instrumentation work was more complicated than the framework instrumentation because of the multi-threaded nature of the converters. Both the offline calorimeter code and the offline tracking code were instrumented in August.

Part of the effort (end of August) has been focused in starting to define the boundaries - within the code - of the relevant benchmarks. This is necessary in order to factorize the critical components of the framework (like data access, etc.).

The first draft of the LVL2 trigger prescaling note was close to being finished at the end of August.